**ALPHA COLLEGE OF ENGGINEERING &TECHNOLOGY**
**FAQ FOR BASIC ELECTRONICS (2110016)**
**DEPARTMENT:CE,IT,EE(2ND SEM)**

CHAPTER 1

1 Explain in brief about Dot Convention.(Dec.2015)

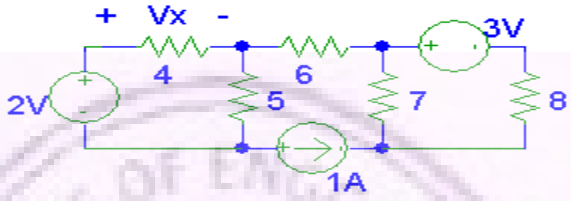
2 Write a short note on Oscilloscope.(Summer-15,Winter 15)

3 Explain in brief about Lumped circuit elements called resistor and capacitor also Write a short note on Ammeter and Voltmeter.(Summer-14)

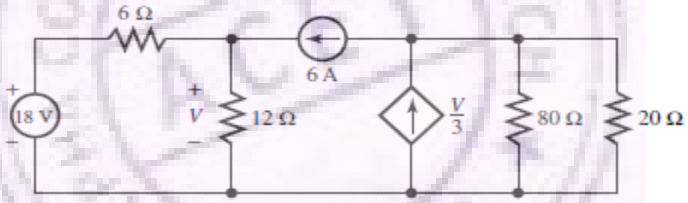
CHAPTER 2

1 Explain DELTA-WYE and WYE-DELTA transformation in brief with necessary equat ions and circuit diagrams .(Summer-14,15)

2 Find the voltage Vx using superposition theorem. All resistor values are in ohm. (Summer-15)




3 Determine the voltage across the 20 Ohm resistor in the following circuit of Figure.(a) with the application of superposition theorem. (Summer-14)




CHAPTER 3

1 Draw circuit diagram of non-inverting operational amplifier & explain in brief. (Summer-15)

2 Describe low pass active filter using Operational amplifier with necessary diagrams and equations. (Summer-15) or Describe band pass active filter using Operational amplifier with necessary diagrams and equations.(Summer-14)

3 Write about Differential amplifier using Op-amp with necessary circuit diagram and equations. (Summer-14)

4 Explain in brief following properties of operational amplifier.
(a) Input Resistance (b) Open Loop Voltage gain
(c) CMRR (d) Input Offset Voltage
(Dec.2015)

CHAPTER 4

1 What is difference between in Microprocessor and Microcontroller?Draw and explain microprocessor system architecture(Summer-15,Winter 15)

2 What do you understand about multiplexing? Explain any one of the Multiplexing technique.( Summer-15)

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3 Reduce the given function using K-map, F=∑m(1,3,5,9,11,13)(Summer-15)

4 Write Short note on D flip flop with circuit diagram and truth table.(Summer-15)
Write Short note on SR flip flop with circuit diagram and truth table.(Summer-14)

5 Classify the types of Computer network? Explain each one of them in brief.(Summer-15)

6 For the switching function F = A(A'+B), draw a corresponding set of logic blocks and write the truth table. *(Summer-14)*

7 Draw only ISO-7 layer model block diagram of an OSI for computer Networks. *(Summer-14)*

8 For the logic expression F=A'B'+AB
(i) Obtain the truth table.
(ii) Name the operation performed
(iii) Realize this operation using AND, OR, NOT gates
(iv) Realize Same operation using only NAND gates (Winter 15)

9 Classify display devices. Also Classify network topologies and draw each one of them (Winter 15)

10 What is transmission medium? What are the different types of transmission medium?(Winter 15)

CHAPTER 5

1 Draw only functional block diagram of signal processing system.(Summer-15)Explain in brief Product Modulation and Demodulation with necessary diagrams.(Summer-15)

2 What do you understand about multiplexing? Explain any one of the Multiplexing technique. (Winter 15)

CHAPTER 6

1 Draw & Explain the functional description of digital communication system in brief.(Summer-15)

2 Classify the s tandard based on 2G & 3G.(Summer-15)

3 Write short not on Cellular communication system.(Summer-14) or Explain in brief cellular concept in mobile radio system.(Winter 15)

4 What do you understand about frequency reuse concept & Why it is used in cellular system?(Summer-15)

5 Draw block diagram of Pulse code Modulation.(Winter 15)

6 Define Waveguide, Transmission lines and Antenna.(Summer-14)

7 Define the following terms:
(a) Reflection (b) Directivity (c) Isotropic Radiator (Winter 15,Summer-15))

8 Compare DSB-FC, DSB-SC, SSB, VSB. (summer 15)

CHAPTER 7

1 Classify the Control systems. (Summer 15) or Compare Open loop and Close loop System.(Summer 15)

2 Explain any four rules of Block diagram reduction for control system with necessary block diagrams. (Summer-14)

3 Draw and explain the typical unit step response (Transient Response) of the control system. (Summer-14)

4 Explain digital control system with necessary block diagrams. (Winter 15)

PAGE NO.
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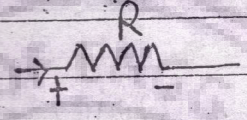
# 1. Circuit concepts

1. Explain lumped circuit parameters.

→ A. Resistance :- can be defined as a characteristic which oppose an electric current.

↳ symbol :- 


↳ $R = \frac{\rho l}{A}$

where, R = Resistance
ρ = Resistivity
l = length
A = Cross section area

↳ Resistivity :- Resistance of a conducto which has unit length and unit cross section area is defined as resistivity.

↳ Voltage drop across resistor :-

$$V = IR$$

↳ Current pass through resistor :-

$$I = \frac{V}{R}$$

↳ If we increase the temperature, resistance of conductor will increase if we increase in temperature resistance of de.

Semiconductor [illegible]

↳ Unit of resistance : ohm → Ω
↳ Unit of resistivity : Ω.m

↳ Conductance $G = \frac{1}{R}$

Unit :- $\Omega^{-1}$ or Siemens.

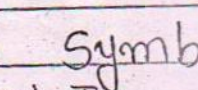
↳ Condyctivity $\sigma = \frac{1}{\text{Resistivity } (\rho)}$

Unit :- $(\Omega m)^{-1}$ or Siemens/me

→ B. Inductor (L) :-

Magnetic flux generated in coil is directly proportional to electric cur

$\Phi \propto I$

→ Symbol :- 


$\therefore \Phi = LI$

$\rightarrow L = \frac{\Phi}{I}$

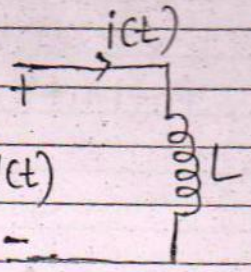
→ Unit :- Henry

L = Inductor
$\Phi$ = Magnetic flux
I = current (Ampere)

↳ Voltage across inductor $V_L = L \frac{d}{d}$

→ An inductor is a dual of capacitor.

→ $di = \frac{1}{L} V(t)\, dt$




$$\therefore i = \frac{1}{L} \int_0^t V(t)\, dt$$

This equation is for an inductor in current.

↳ Energy stored in Inductor :-

$$E_L = \int P_L\, dt$$

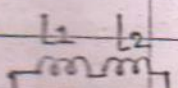
$$= \int (V_L \cdot I_L)\, dt$$

$$= \int L \cdot \frac{di}{dt} \cdot I_L\, dt$$

$$= L \int I_L\, di$$

$$= L \frac{I^2}{2}$$

$$E_L = \frac{1}{2} L I^2$$




↳ Series Connection : $L_{eq} = L_1 + L_2 + L_3 + \ldots$

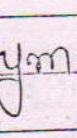

↳ Parallel Connection : $\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2} + \ldots \frac{1}{L_n}$

PAGE NO.
DATE

## C. Capacitor (C) :-

Electric charge stored per unit potential difference is called capacitance

→ Capacitance $\boxed{C = \frac{Q}{V}}$

→ Symbol :- 


→ $C = \frac{\varepsilon_0 A}{d}$

where, A = area of plate
d = distance between two plates
$\varepsilon_0$ = permittivity

→ Current through capacitor :-

$Q = C \times V$

$\therefore I = \frac{dQ}{dt}$

$\boxed{I_c = C \frac{dV}{dt}}$

→ Voltage across capacitor :-

$I = C \frac{dV}{dt}$

$\therefore V = \frac{1}{C} \int I dt$ $\quad \boxed{\therefore dV = \frac{I}{C} dt}$

→ Energy stored by capacitor :-

$$E_c = \int P_c \, dt$$

$$= \int V_c \cdot I_c \, dt$$

$$= \int V_c \cdot C \cdot \frac{dV}{dt} \cdot dt$$

$$= C \int V_c \cdot dV$$

$$= C \frac{V^2}{2}$$

$$\boxed{E_c = \frac{1}{2} C V^2}$$

→ Unit of capacitance :- Faraday (F)

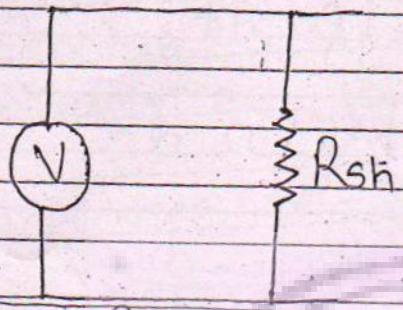
## (2) Meters and Measurements :-

### 1. Voltmeter :

→ Measure - Voltage / Potential diff.
→ Connection - parallel
→ Symbol - Ⓥ

→ A.C. - r.m.s. Value
DC - de value

→ Practical Voltmeter




Ideally $R_{sh} = \infty$

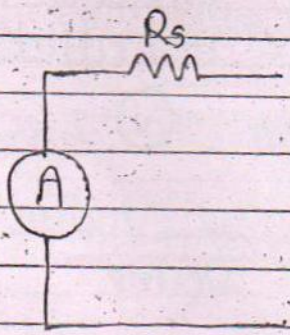
where, $R_{sh}$ = shunt internal Resistance

## 2. Ammeter :-

→ Measure - Current
→ Connection - Series
→ Symbol - —(A)—

→ AC - R.M.S. Current
DC - d.c. current

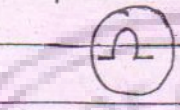
→ Practical Ammeter




$R_g$ = Series internal Resistance

Ideally $R_s = 0$

## 3. Ohmmeter :-

→ Measure :- Resistance
→ Connection :- Parallel
→ Symbol :- 
→ Ac → dynamic R dV/dt
→ DC → static R V/I

## 4. Multimeter :-

→ Measure :- Resistance → Parallel
current (Ac/dc) → series
Volteige (Ac/dc) → Parallel

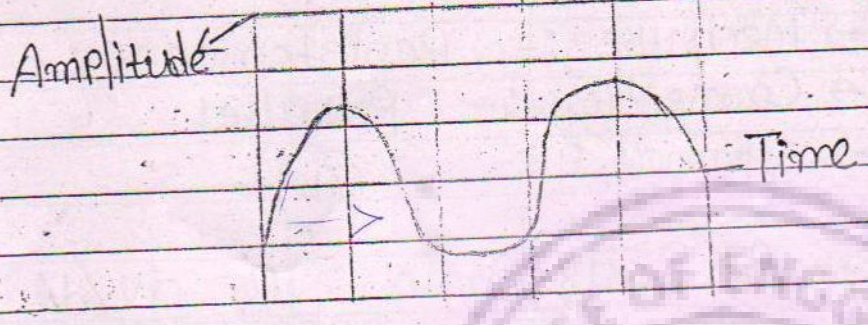
→ V O M
(Volt ohm Mili Ampere)

→ Types :-
1. Analog Multimeter
2. Digital Multimeter

## 5. CRO :-

→ cathode ray oscilloscope

→ Time Varing quantities




6. Galvanometer :-

→ Detect the current

7. Instrumental transformers :-

1. potential transformer (P.T.)

2. Current transformer (C.T.)

1. P.T. is basically step down transform.

$$V_2 = V_1 \times \frac{N_2}{N_1}$$

2. C.T. is basically step up transformer.

$$I_2 = I_1 \times \frac{N_1}{N_2}$$

$N_2 >> N_1$

Current is measured in Ammeter.

PAGE NO.
DATE

3) Difference between Hydraulic & Electr

| Hydraulic | | Electric |
|---|---|---|
| Fluid (water) | → | charge |
| flow of water | → | current |
| Level of water | → | Potential |
| capacity of tank | → | Capacitance |

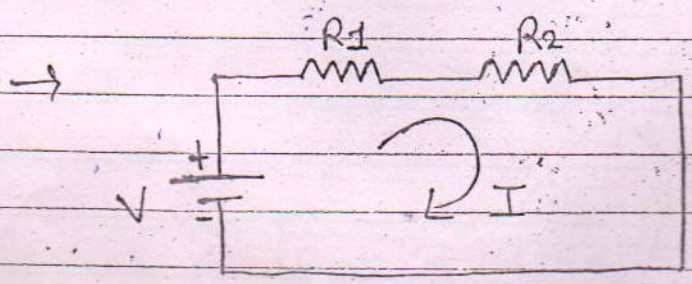
→ Difference between Thermal & Electric

| Thermal | | Electric |
|---|---|---|
| Heat | → | charge |
| flow of Heat | → | current |
| Temp difference | → | Potential |
| heat capacity | → | capacitance |
| Thermal resistance | → | resistance |

(4) Kirchoff's Voltage law :-

Algebraic sum of Voltage in closed loop is always = 0.

$$\Sigma V = 0$$



→ According to KVL

Voltage drop across
$V_1 = IR_1$

Voltage drop across
$V_2 = IR_2$

→ According to KVL

$V - V_1 - V_2 = 0$

$\therefore V - IR_1 - IR_2 = 0$

$\therefore V = IR_1 + IR_2$

→ KVL is generally used to calculate the unknown currents in a ckt.

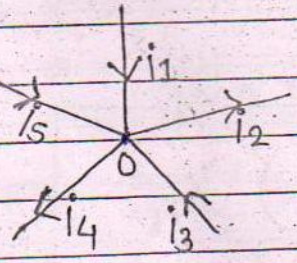
→ KVL is Proof of energy conservation law.

* Kirchoff's Current law :-

Algebraic sum of current at node = 0.

$$\boxed{\Sigma I = 0}$$

→



Here, 5 branches have Connected node 0.

Assume outgoing current as positive current according to KCL.

KCL $-i_1 + i_2 - i_3 + i_4 - i_5 = 0$

$i_2 + i_4 = i_1 + i_3 + i_5$

→ KCL is used for obtaining the unknown Volteges in the given network.

→ KCL is proof of charge conservation law.

5. Coulomb's law :-

(1) 1. Like charges ~~attraction~~ Repulsion
2. Unlike charges ~~Unattraction.~~ ~~Repulsion~~ attraction

(2) Second (Coulomb's inverse law)

→ Coulomb force between two charges is directly proportional to multiplicatio of charge & inversely proportional to square of the between them.

$$F \propto \frac{q_1 q_2}{r^2}$$

$$\boxed{F = K \frac{q_1 q_2}{r^2}}$$

$$K = \frac{1}{4\pi\varepsilon_0}$$

$$\boxed{\varepsilon_0 = 8.85 \times 10^{-12} \ F/m}$$

5. Define the following terms :-
(equations & Unit)

1. Electric current :-

$$\boxed{I = Q/t}$$

Flow of free electric charge per unit time is defined as electric current.

I = Ampere
Q = Coulomb
t = second

$$\text{Ampere} = \frac{\text{Coulomb}}{\text{second}}$$

2. Energy / workdone :-
Ability to do work is defined as energy.

$$\boxed{E = P \times t}$$

Unit :- Joule or N.m or w-h

3. Electric Field :-

$$\boxed{E = F/q}$$

Coulomb force per unit charge is defined as electric field.

$F = N$

$Q = C$

Unit :- N/C

4. Electric Potential :-

$$V = \frac{\text{Workdone}}{\text{charge}}$$

workdone per unit charge to move it from 1 point to another point in electric field is defined as electric potential.

Unit :- J/C

Volt = J/C

5. Power :-

$$P = \frac{E}{t}, \quad P = V \times I$$

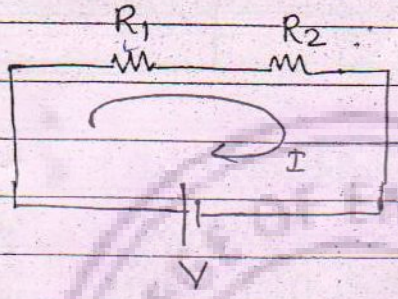
Energy used per unit time is defined as power.

watt = J/s

Unit = W, J/s

* Derive the equation for series and Parallel connection of Resistor.

Series :-



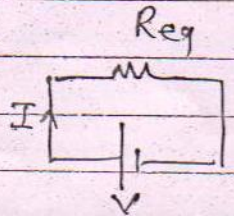

Here Resistence $R_1$ and $R_2$ are connected in series with battery V. current passing from this ckt is I. In series connection of Resistors current is same for all the resistors.

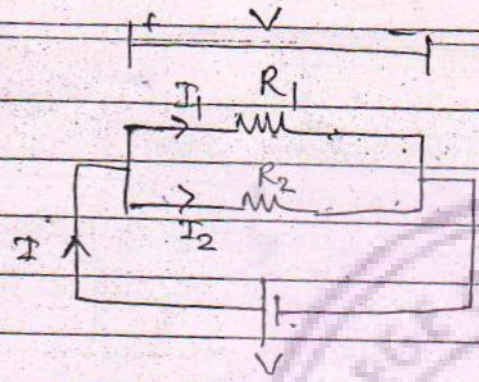
So Volteye drop across $R_1 = V_1 = IR_1$
" " " $R_2 = V_2 = IR_2$

According to KVL

$$V - V_1 - V_2 = 0$$
$$\therefore V = V_1 + V_2$$
$$\therefore V = I(R_1 + R_2)$$
$$\therefore \frac{V}{I} = R_1 + R_2$$
$$\therefore R_{eq} = R_1 + R_2$$

where $\frac{V}{I} = R_{eq}$ $\longrightarrow$






Here resistor $R_1$ and $R_2$ are connected in parrallel connection with batery. Current passing from $R_1$ is $I_1$ and current passing from $R_2$ is $I_2$. Volteye is simuler in parallel connetion for both resistor.

According to KCL,

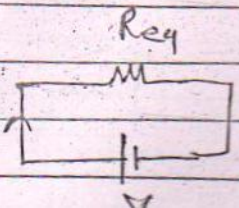
$$I = I_1 + I_2$$

$$\therefore I = \frac{V}{R_1} + \frac{V}{R_2}$$

$$\therefore \frac{I}{V} = \frac{1}{R_1} + \frac{1}{R_2}$$

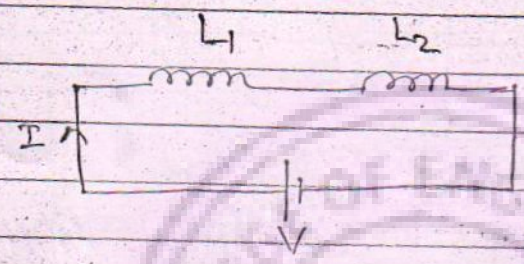
$$\therefore \boxed{\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2}}$$

Where $R_{eq} = \frac{V}{I}$



* Derive the equation for series and parallel connection of inductor.

Series:-




Here inductors $L_1$ and $L_2$ are connected in series connection with batery V. Current passing through ckt is I. Current is similar in series connection of Resistors.

Voltage across inductor $L_1 = V_1 = L_1 \frac{dI}{dt}$

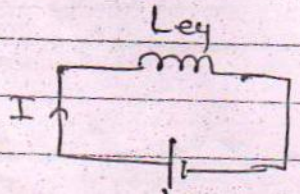
" " " $L_2 = V_2 = L_2 \frac{dI}{dt}$

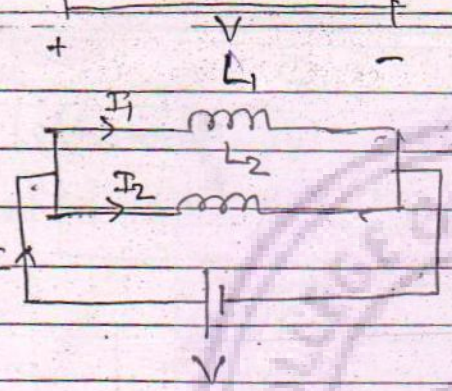
According to KVL,

$$V = V_1 + V_2$$

$$\therefore L_{eq} \frac{dI}{dt} = L_1 \frac{dI}{dt} + L_2 \frac{dI}{dt}$$

$$\therefore \boxed{L_{eq} = L_1 + L_2}$$





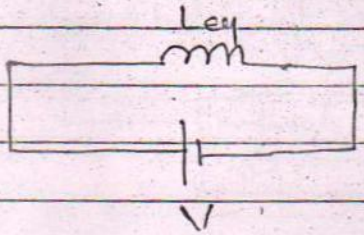

Here inductor $L_1$ and $L_2$ are connected in parallel with batery V. Current passing from $L_1$ is $I_1$ and current passing from $L_2$ is $I_2$. Voltage is similer in parallel connection.

Acording to KCL,

$$I = I_1 + I_2$$

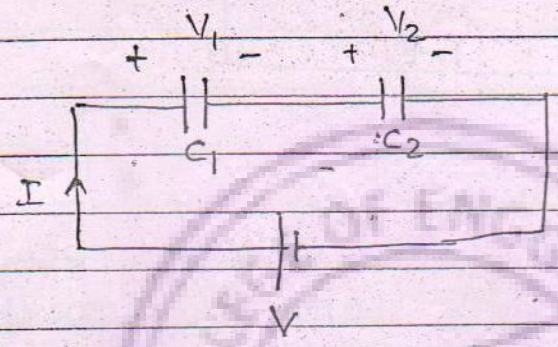
$$\therefore \frac{1}{L_{eq}} \int V\,dt = \frac{1}{L_1} \int V\,dt + \frac{1}{L_2} \int V\,dt$$

$$\therefore \boxed{\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2}}$$



* Derive the equation for parallel and series connection of capacitor:-

Series:




Here capacitor $C_1$ and $C_2$ are connected in series with batery V. and current passi From circuit is I. Current is simular for both capacitor.

Voltage across capacitor $C_1 = V_1 = \frac{1}{C_1}\int I\,dt$

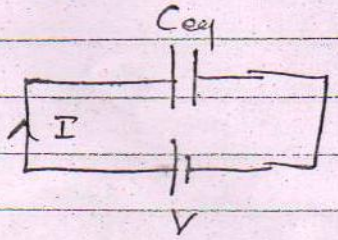
" " " $C_2 = V_2 = \frac{1}{C_2}\int I\,dt$

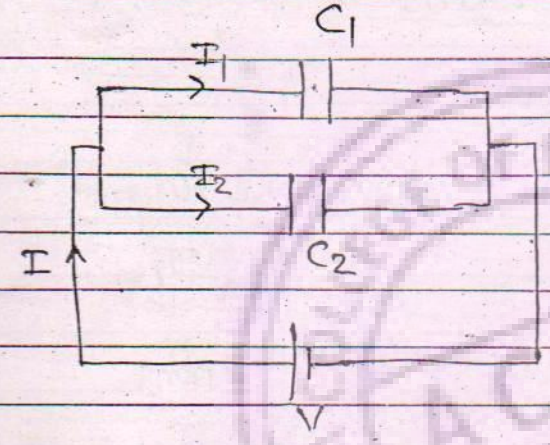
acording to KVL,

$$V = V_1 + V_2$$

$$\therefore \frac{1}{C_{eq}}\int I\,dt = \frac{1}{C_1}\int I\,dt + \frac{1}{C_2}\int I\,dt$$

$$\therefore \boxed{\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}}$$





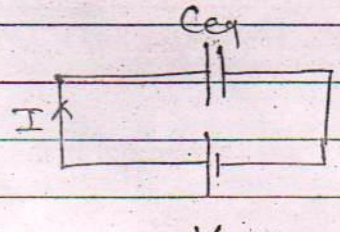

Here capacitor $C_1$ and $C_2$ are connected in parallel with batery V. Current passing from $C_1$ is $I_1$ and current passing from $C_2$ is $I_2$. Voltage is similar for both capacitor.

According to KCL,

$$I = I_1 + I_2$$

$$\therefore C_{eq} \frac{dV}{dt} = C_1 \frac{dV}{dt} + C_2 \frac{dV}{dt}$$

$$\therefore \boxed{C_{eq} = C_1 + C_2}$$



PAGE NO.
DATE

| Mechanical system | Vs | Electrical system |
|---|---|---|
| | Force-current Analogy | Force-Voltage Analogy |
| Force | Current | Voltage |
| Velocity | Voltage | Current |
| Mass | Capacitance | Inductance |
| Compliness | Inductance | Capacitance |
| Friction or Damping | Conductance | Resistance |

# 4. Digital Building Blocks



Aneri Pandya.
BE-

Ch-4

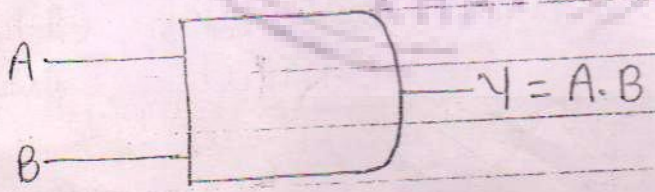
## 1. Basic logic gates :-

### (1) Not :-


| A | Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

→ The NOT gate is also known as an "Inverter" because its output is the inverted version.

### (2) AND -




Truth table :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

→ AND is one of the logic operators. It performs the logical multiplication on its inputs. The output is high when inputs are high(1).

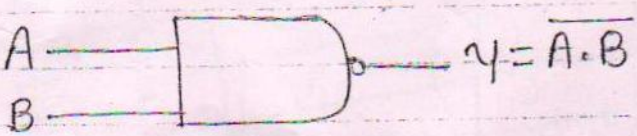
(3) OR gate :-


Truth table :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

→ An "OR" gates performs the logical addition on its inputs therefore it output will be high (1) if any or or both the inputs are high (1).

4. NAND (AND + NOT) :-




Truth table :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

→ A NAND gate is cal
as "Universal Gate" b'c
we can construct AN
OR and NOT gates usi
only NAND gates.

5. NOR (OR + NOT) :-

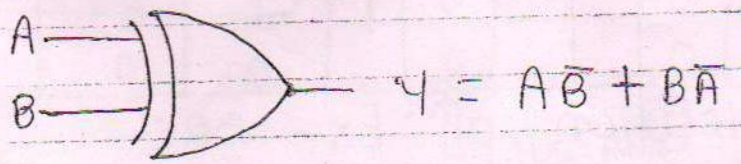

Truth table :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

→ NOR gate is called as "universal gate" because we can construct AND, OR and NOT gates using only NOR gate.

6. Ex - OR

→




↳

| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

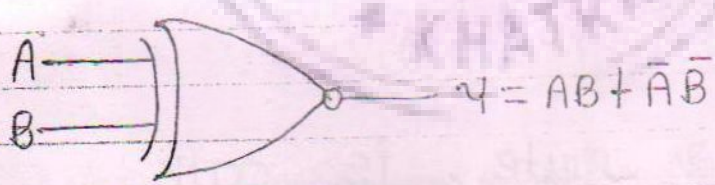
The exclusive OR gate is abbreviated as EX-OR gate or X-OR gate.

$Y = A \oplus B$ or $A\bar{B} + B\bar{A}$

→ Application of Ex-OR :-

1. As a magnitude comparator
2. In the binary to gray code converter.
3. In the adder and subtractor circuits.
4. In the parity generator.
5. As a modulo-2 adder.

7. Ex-NOR :-




| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

→ The word Ex-NOR is a short form of exclusive -NOR.

→ $Y = \overline{A \oplus B}$ or $Y = AB + \bar{A}\bar{B}$

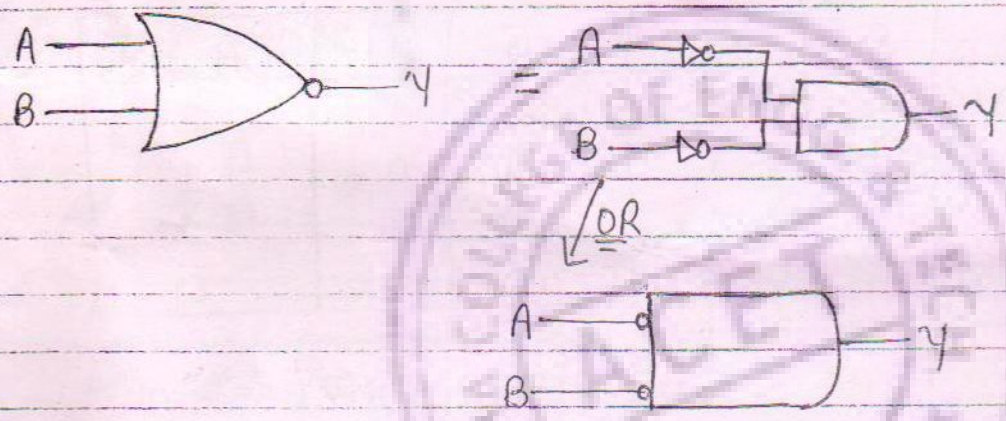
→ Application of Ex-NOR :-

1. As even Parity generator.
2. As a comparator.
3. As even parity checker.

2. State and Prove d'morgan's law.-

1. $\overline{A+B} = \bar{A} \cdot \bar{B}$

NOR = Bubbled And gate



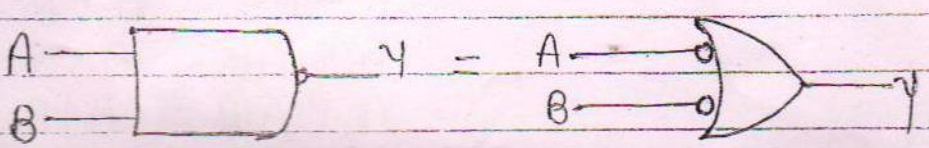

Truth table :-

| A | B | $\bar{A}$ | $\bar{B}$ | $\overline{A+B}$ | $\bar{A} \cdot \bar{B}$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |

L.H.S. = R.H.S.

2. $\overline{A \cdot B} = \bar{A} + \bar{B}$

NAND = Bubbled OR



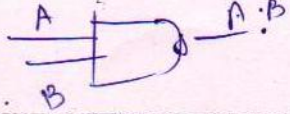
→ This theream states that the, comple of a product is equal to additio of the complements.

→ Truth table :-

| A | B | $\bar{A}\bar{B}$ | $\bar{A}$ | $\bar{B}$ | $\bar{A}+\bar{B}$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |

## :- Boolean expression :-

| Sr No. | Name | Statement of the law |
|---|---|---|
| 1. | Commutative Law | $A.B = B.A$<br>$A+B = B+A$ |
| 2. | Associative Law | $(A.B).C = A.(B.C)$<br>$(A+B)+C = A+(B+C)$ |
| 3. | Distributive Law | $A.(B+C) = AB+AC$ |
| 4. | AND Laws | $A.0 = 0$ \| $A.A = A$<br>$A.1 = A$ \| $A.\bar{A} = 0$ |
| 5. | OR Laws | $A+0 = A$<br>$A+1 = 1$ \| $A+\bar{A} = 1$<br>$A+A = A$ |
| 6. | Inversion Law | $\bar{\bar{A}} = A$ |
| 7. | other Important Laws | $A+BC = (A+B)(A+C)$<br>$\bar{A}+AB = \bar{A}+B$<br>$\bar{A}+A\bar{B} = \bar{A}+\bar{B}$<br>$A+AB = A$<br>$A+\bar{A}B = A+B$ |




PAGE NO.
DATE

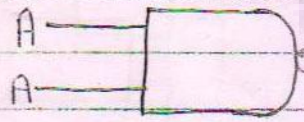
## Explain NAND gate as universal gate:-

→ NAND gate can be used as universal gate b' coz any of the gate can be design by NAND gate only.

→ (1) NOT gate

$Y = \overline{A}$

$= \overline{A \cdot A}$



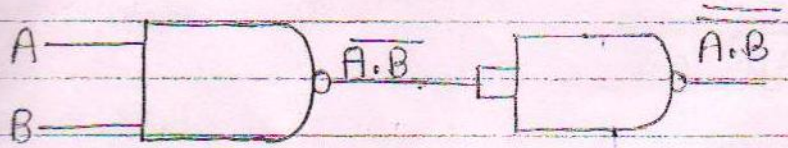

=


(2) AND gate

NAND = AND + NOT.

$Y = A \cdot B$

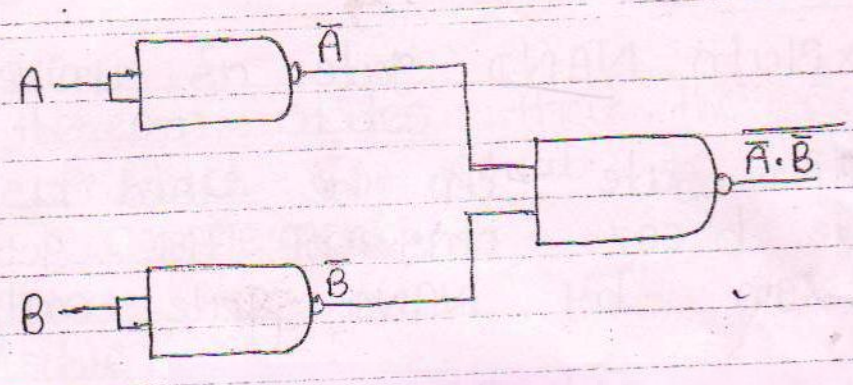
$= \overline{\overline{A \cdot B}}$




(3) OR gate

$Y = \overline{\overline{A + B}}$

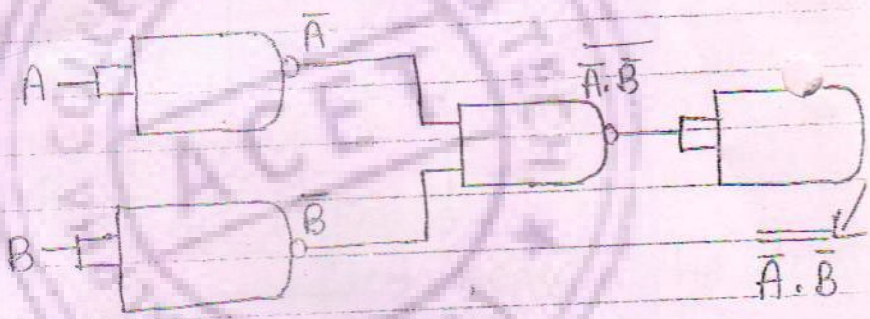
$Y = \overline{\overline{A} \cdot \overline{B}}$




## (4) NOR gate :-

$Y = \overline{A+B}$

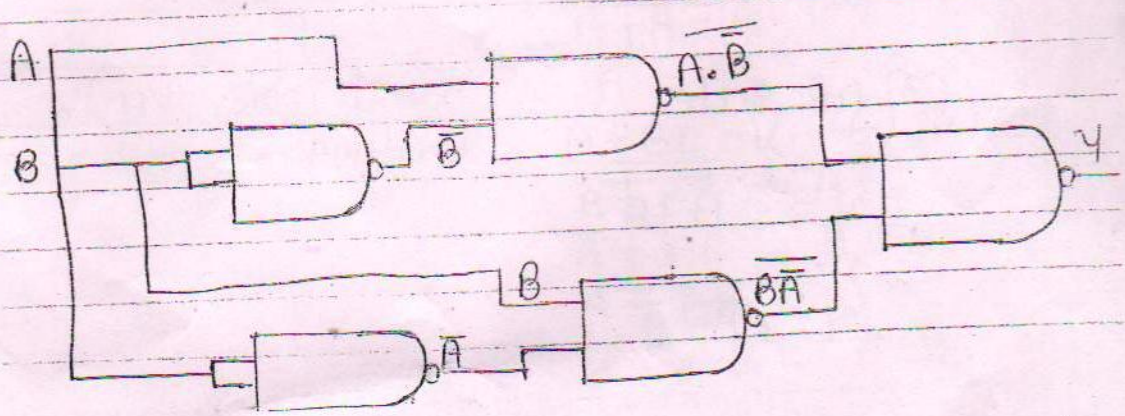
$Y = \overline{\bar{A}.\bar{B}}$




## (5) Ex-OR gate :-

$Y = \overline{A\bar{B} + B\bar{A}}$

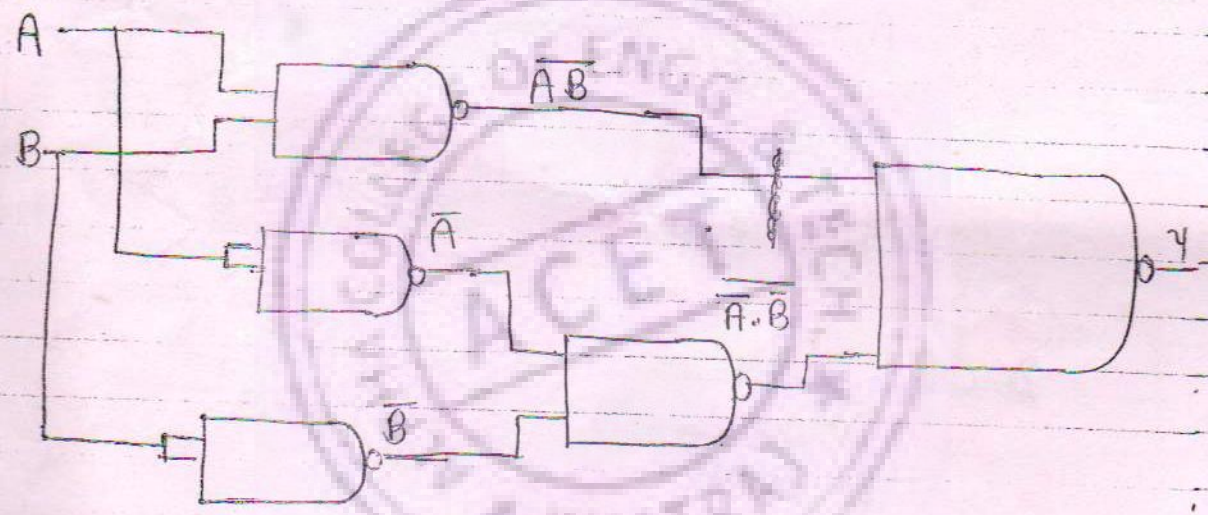
$Y = \overline{\overline{A\bar{B}}.\overline{B\bar{A}}}$



Ex-NOR

$$Y = A\bar{B} + \bar{A}B$$

$$Y = \overline{\overline{A\bar{B}} \cdot \overline{\bar{A}B}}$$



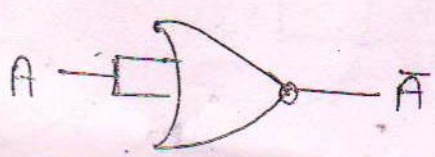

4. Explain NOR gate as universal gate:-

→ NOR gate can be used as universal gate b'coz any gate can be design by NOR gate.

1. NOT gate

$$Y = \bar{A}$$

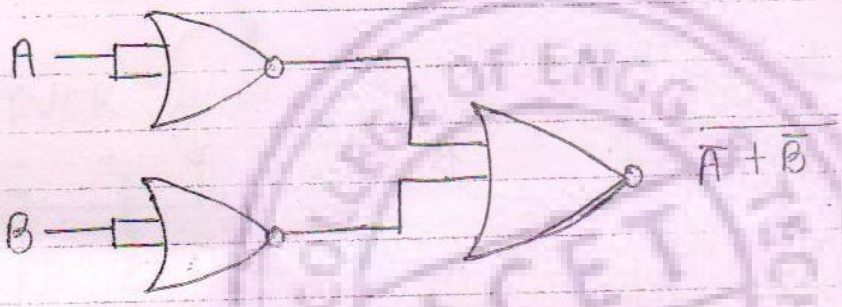
$$Y = \overline{A+A}$$



2. AND gate :-

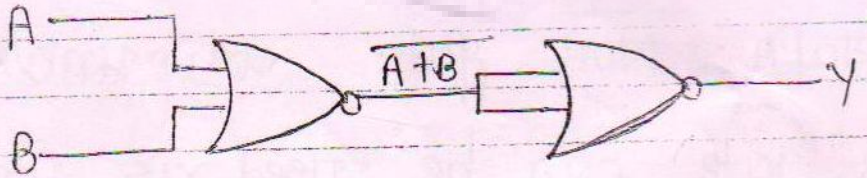
$Y = \overline{\overline{A} + \overline{B}}$

$Y = \overline{\overline{A} + \overline{B}}$



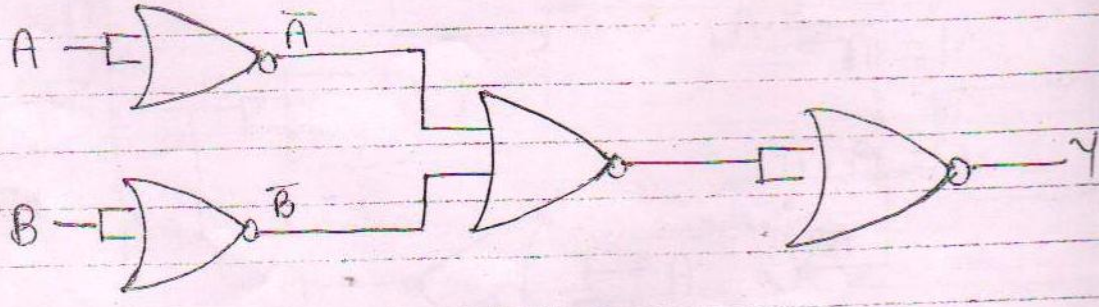

3. OR gate :-

$Y = \overline{\overline{A + B}}$




4. NAND gate :-

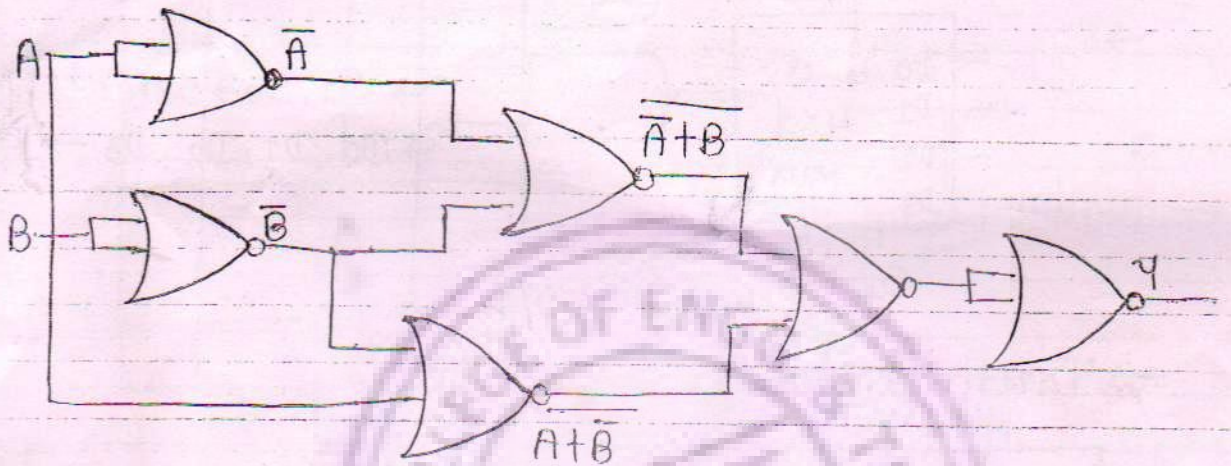
$Y = \overline{A \cdot B} = \overline{\overline{A} + \overline{B}}$



Ex-OR gate :-

$$Y = A\bar{B} + B\bar{A}$$

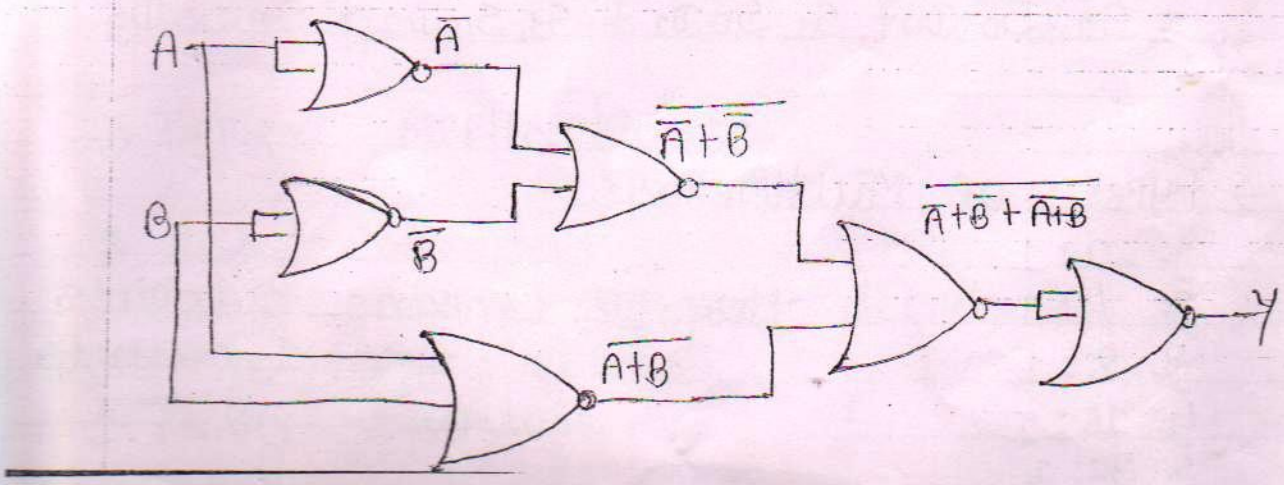
$$Y = \overline{\bar{A}+B} + \overline{\bar{B}+A}$$




6. Ex-NOR :-

$$Y = AB + \bar{A}\bar{B}$$

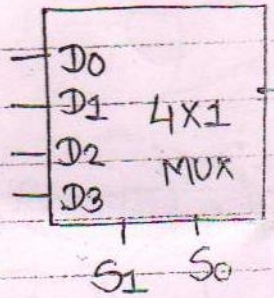
$$= \overline{\bar{A}+\bar{B}} + \overline{A+B}$$



## 5. Explain 4x1 Multiplexor :-

→ Multiplexor is also called data selector. Multiplexor is a special type of combinational circuit.

→




↳ $S_1, S_0$ → Select line
↳ $D_0, D_1, D_2, D_3$ → Input

→ Truth table

| $S_1$ | $S_0$ | Y |
|---|---|---|
| 0 | 0 | $D_0$ |
| 0 | 1 | $D_1$ |
| 1 | 0 | $D_2$ |
| 1 | 1 | $D_3$ |

→ ckt diagram:-

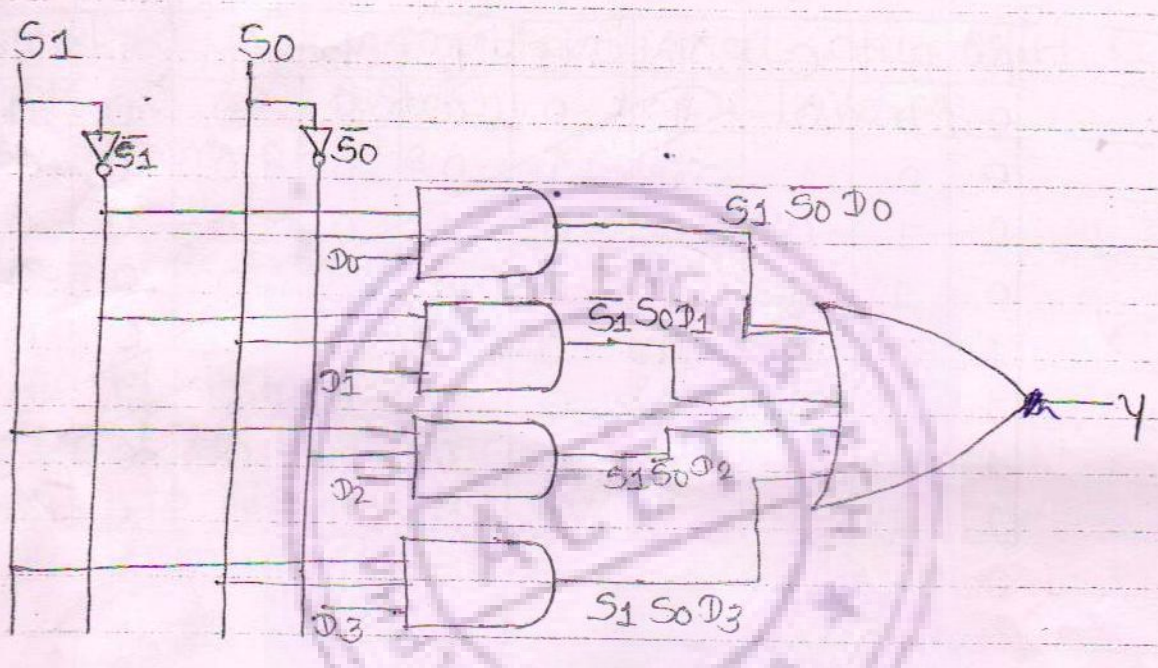
$= \overline{S_1}\,\overline{S_0}\,D_0 + \overline{S_1}\,S_0\,D_1 + S_1\,\overline{S_0}\,D_2 + S_1\,S_0\,D_3$

→ Types of Multiplexors:-

1. 2:1
2. 4:1
3. 8:1
4. 16:1
5. 32:1

Here, 2:1 means 2 inputs and 1 outputs

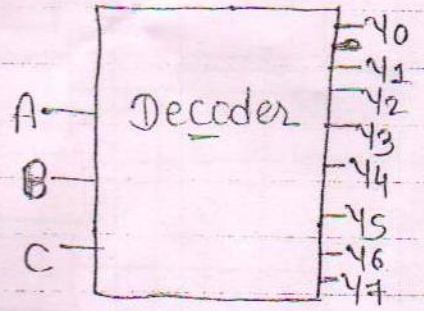
ckt :-




6. Explain 3:8 Decoder :-

→ A decoder is a combinational circuit.

→




n = inputs

$Y = 2^n$

→ Typical Applications :-

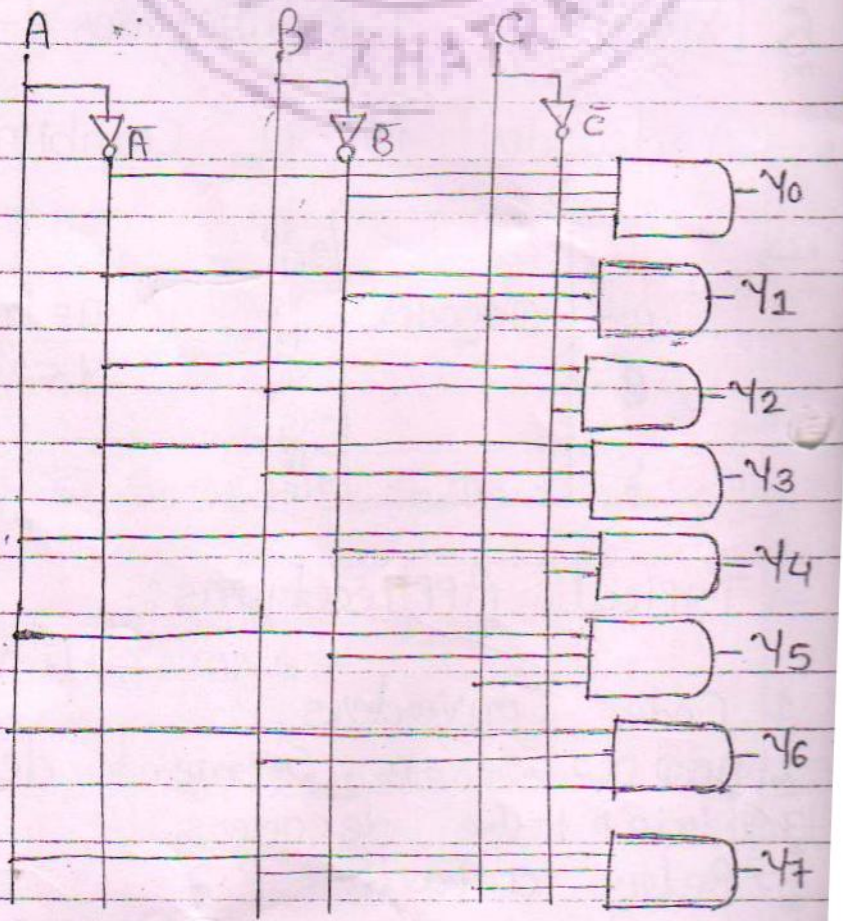
1. Code Converters
2. BCD to seven segment decoders.
3. Nixie tube decoders.
4. Relay actuators.

→ Truth table :-

| A | B | C | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

→ Ckt diagram :-

$Y_0 = \bar{A}\bar{B}\bar{C}$
$Y_1 = \bar{A}\bar{B}C$
$Y_2 = \bar{A}B\bar{C}$
$Y_3 = \bar{A}BC$
$Y_4 = A\bar{B}\bar{C}$
$Y_5 = A\bar{B}C$
$Y_6 = AB\bar{C}$
$Y_7 = ABC$



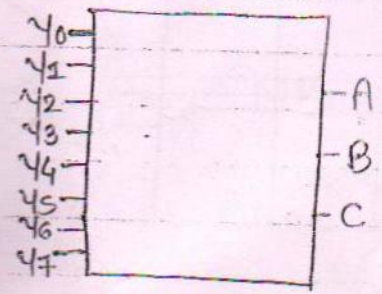
Explain 8:3 Encoder :-

→ Encoder is a combinational ckt which is designed to perform the inverse operation of the decoder.

→ Types of Encoders :-

1. Priority encoders
2. Decimal to BCD encoder
3. Octal to Binary encoder
4. Hexadecimal to binary encoder.

→




→

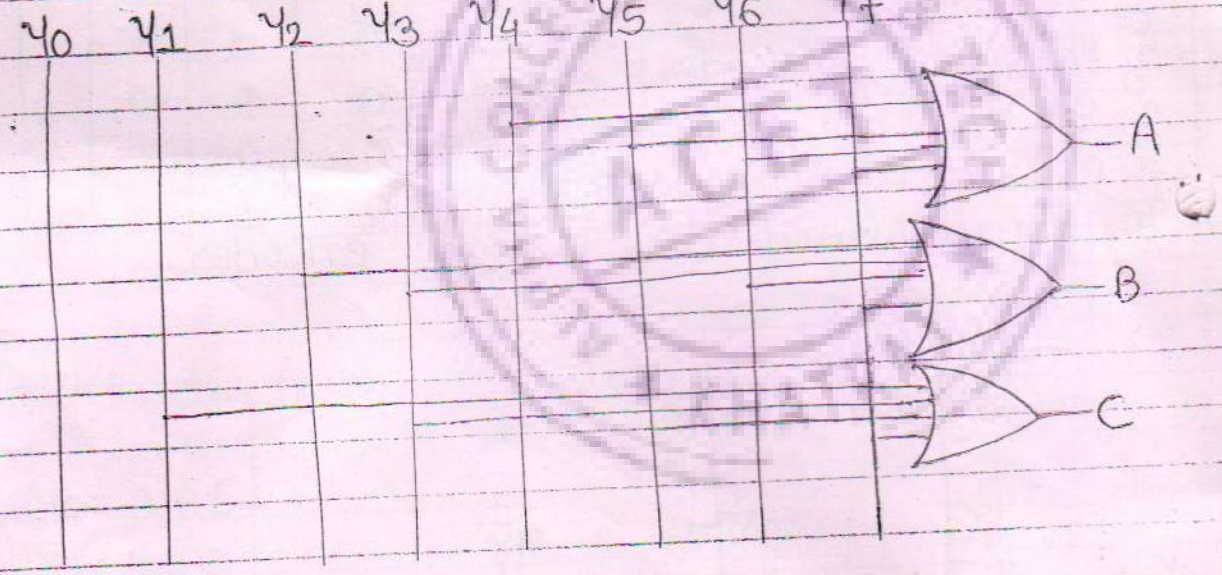
| Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | A | B | C |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

→ only encoder use this method :-

$A = Y_4 + Y_5 + Y_6 + Y_7$

$B = Y_2 + Y_3 + Y_6 + Y_7$

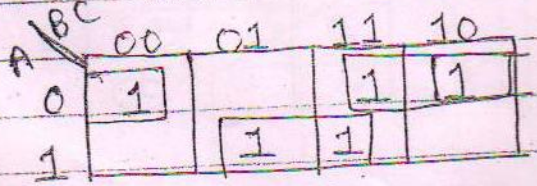
$C = Y_1 + Y_3 + Y_5 + Y_7$




## * K-map Examples [Minimization of eqn :-]

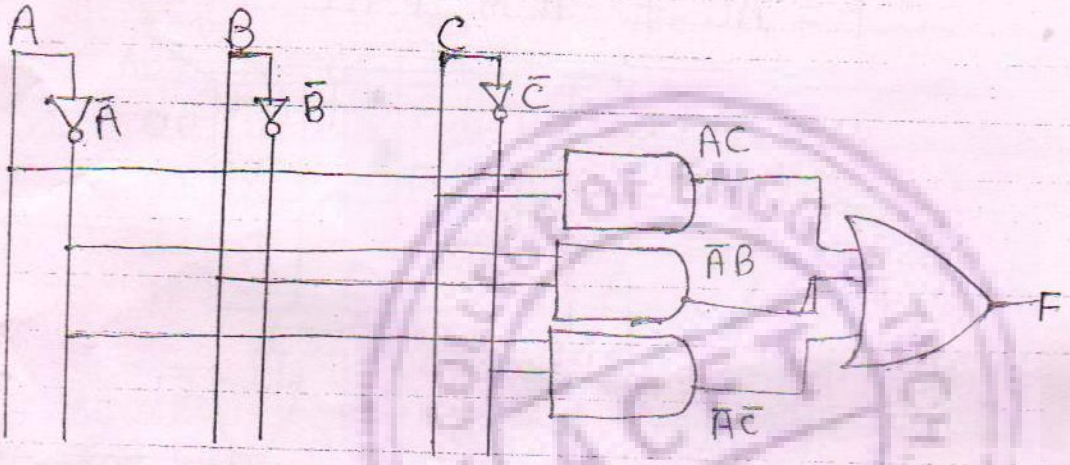
1. Design the circuit using only NAND gate

(1) $F(A,B,C) = \Sigma m\,(0, 2, 3, 5, 7)$
000 010 011 101 111



$F = AC + \bar{A}B + \bar{A}\bar{C}$

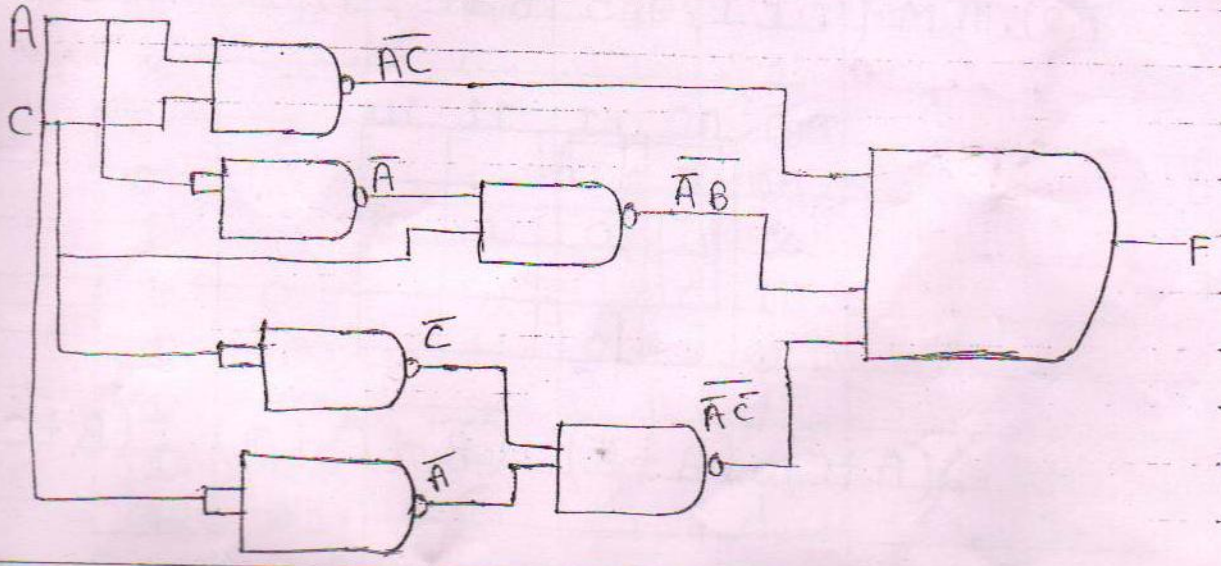
(a) using any gate :-




(b) using NAND gate only :-

$$F = AC + \bar{A}B + \bar{A}\bar{C}$$

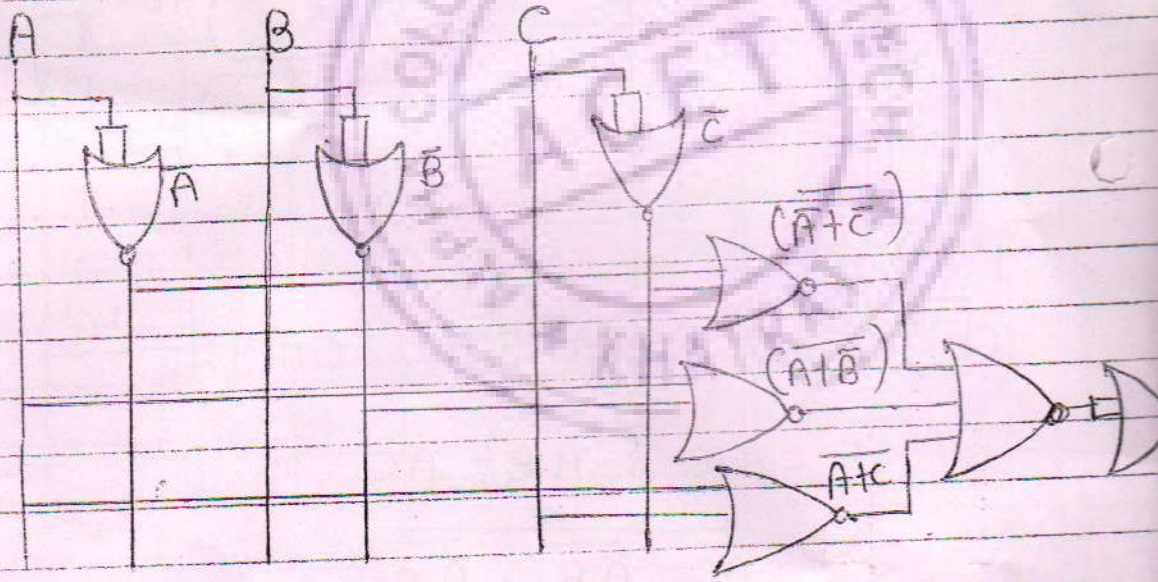
$$= \overline{\overline{AC} \cdot \overline{\bar{A}B} \cdot \overline{\bar{A}\bar{C}}}$$



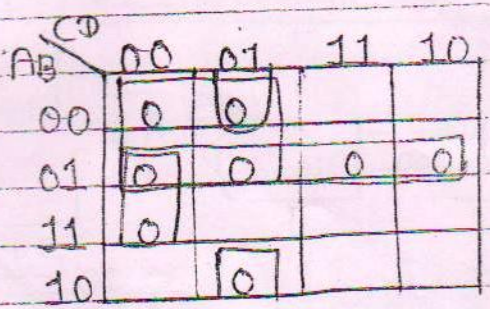
Using only NOR gate:-

$$F = \overline{\overline{AC} + \overline{\overline{A}B} + \overline{A\overline{C}}}$$

$$= \overline{\overline{A}+\overline{C}} + \overline{A+\overline{B}} + \overline{A+C}$$




(2) $\Pi M(0, 1, 4, 5, 6, 7, 9, 12)$




$$(A+C)\cdot(A+\overline{B})\cdot(\overline{B}+C+D)\cdot(B+C+\overline{D})$$

$\Pi M$ (max term e.g. (1,4,7)) POS Form

$\Sigma m$ (min term e.g. (1,5,9)) SOP

PAGE NO.
DATE

3. $F(A,B,C,D) = \Sigma m(0,1,5,6,12,14,15) + d(2,3,4,7)$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | X | X |
| 01 | X | 1 | X | 1 |
| 11 | 1 | | 1 | 1 |
| 10 | | | | |

* A Boolean function $F(A,B,C,D)$ is specified by the truthtable as shown in Figure. obtain minimum SOP form and minimum POS Form.

| 8 A | 4 B | 2 C | 1 D | F | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | ✓ |
| 0 | 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 0 | 0 | |
| 0 | 0 | 1 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 1 | ✓ |
| 0 | 1 | 0 | 1 | 1 | ✓ |
| 0 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 1 | 0 | |
| 1 | 0 | 0 | 0 | 1 | ✓ |
| 1 | 0 | 0 | 1 | 0 | |
| 1 | 0 | 1 | 0 | d | |
| 1 | 0 | 1 | 1 | d | |
| 1 | 01 | 0 | 0 | d | |
| 1 | 01 | 0 | 1 | d | |

| A | B | C | D | F |
|---|---|---|---|---|
| 1 | 1 | 1 | 0 | d |
| 1 | 1 | 1 | 1 | d |

$\sum m(0,4,5,8) + d(10,11,12,13,14,15$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | | | |
| 01 | 1 | 1 | | |
| 11 | d | d | d | d |
| 10 | 1 | | d | d |

$F = \bar{C}\bar{D} + B\bar{C}$ → SOP

$\prod m(1,2,3,6,7,9) + d(10,11,12,13,14,1$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 0 | 0 | 0 |
| 01 | | | 0 | 0 |
| 11 | d | d | d | d |
| 10 | | 0 | d | d |

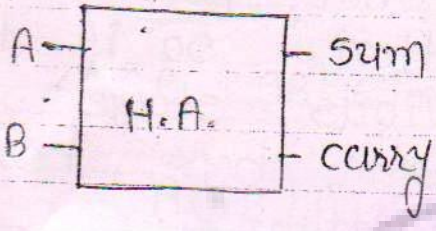
$F = \bar{C}.(B + \bar{D})$ → POS

d or X → Don't care

PAGE NO.
DATE

Explain Half adder with ckt diagram what are the disadvantages of adder.

→




→ Half adder is use to perform 2 bit addition. so, it has 2 inputs and 2 outputs of Half adder are sum and carry.

→ Truth table

| A | B | sum | carry |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

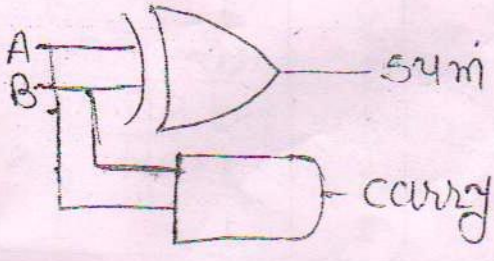
10

→ Boolean equation:-

$$Sum = A\bar{B} + \bar{A}B$$
$$= A \oplus B$$

$$carry = AB$$

→ ckt design



→ Disadvantage of Half Adder :-

Half Adder can not perform more th two bit addition so if there is carry in previous stage, Addition can not perform by half adder.

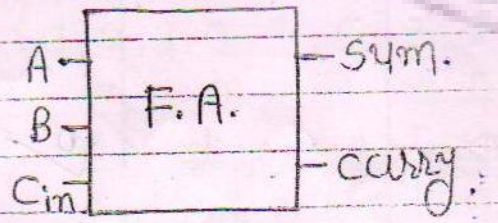
e.g. 3 bit addition

$$\begin{array}{r} \overset{1}{0}\ 1 \\ +\ 0\ 1 \\ \hline 1\ 0 \end{array}$$

so, to perform more than 2 bit addition we have to use full adder

10. Explain Full adder with ckt diagram

→




→ Truth table :-

| A | B | Cin | Sum | carry |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Boolean expression:-

Sum = $\bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

$= (\bar{A}\bar{B} + AB)C_{in} + (\bar{A}B + A\bar{B})\bar{C}_{in}$

$= \underbrace{(A \odot B)}_{\bar{a}} C_{in} + \underbrace{(A \oplus B)}_{a} \bar{C}_{in}$

$\bar{a}C + a\bar{C}$

$= a \oplus C_{in}$

$= A \oplus B \oplus C_{in}$

Carry = $AB\bar{C}_{in} + A\bar{B}C_{in} + \bar{A}BC_{in} + ABC_{in}$

$= AB\bar{C}_{in} + A\bar{B}C_{in} + BC_{in}(\bar{A} + A)$

$= \underline{AB}\bar{C}_{in} + A\bar{B}C_{in} + \underline{BC}_{in}$

$= B(A\bar{C}_{in} + C_{in}) + A\bar{B}C_{in}$

$= B(A + C_{in}) \cdot (\underline{\bar{C}_{in} + C_{in}}) + A\bar{B}C_{in}$

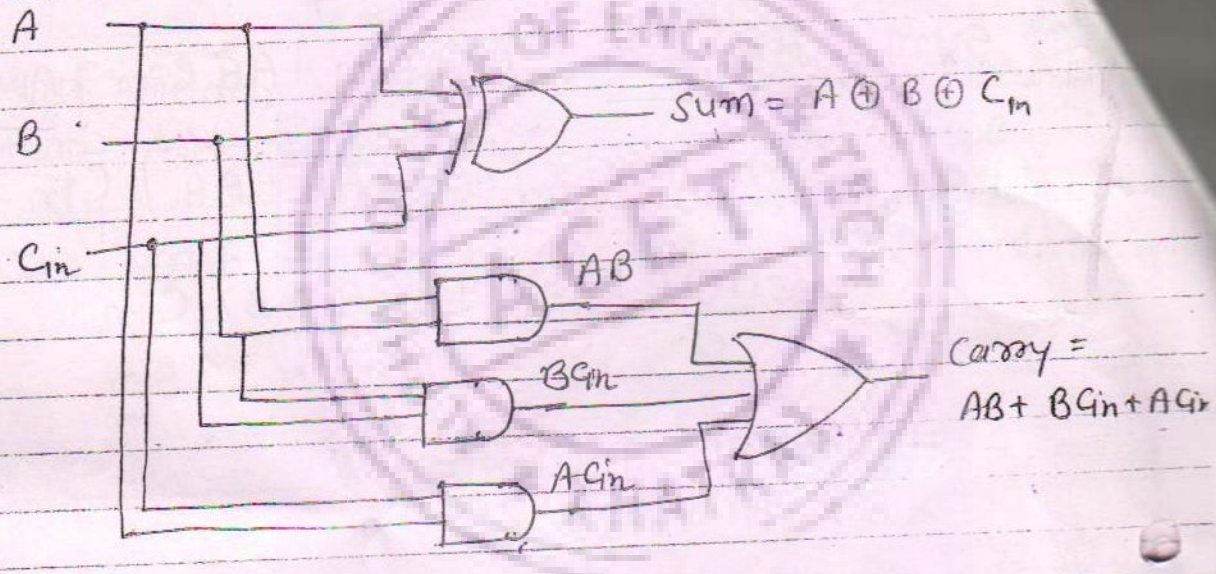
$= AB + BC_{in} + A\bar{B}C_{in}$

$= AB + C_{in} \cdot (B + A\bar{B})$

$= AB + C_{in}(B + \bar{B} \cdot (B + A))$

$= AB + BC_{in} + AC_{in}$ → =1

antage:- Perform more than 2 bit addition as 3 bit addition we have to use full adder.




* The following questions you have to read from books.

(1) Number system conversion. (Binary, Octal, decimal, Hexa)
(2) Ckt desiging using gates
(3) BCD, Excess-3, gray code
(4) Explain the following flipflops (Most Imp)
S-R, J-K, D, T, Masterslave
(5) OSI layer (Networking of Computer) (Imp)
(6) Network topologies
7) Microprocessor & Controller
8) display devices.
9) Types of Networks.

BCD code:- (Binary coded decimal)

$(13)_{10} = (0001\ 0011)_{BCD}$

Excess-3 = BCD + 3

$(13)_{10} = (0100\ 0110)_{EX-3}$

```
  1  3
+ 3  3
  4  6
```

0100 → 4, 0110 → 6

$(99)_{10} = (\quad)_{EX-3}$

[CC] $(1100\ 1100)_{EX-3}$

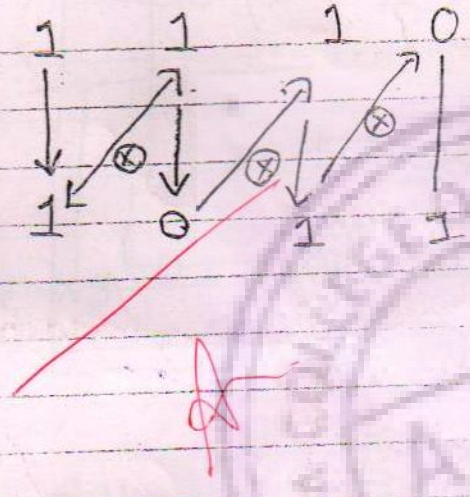
$(1100)_2 = (\quad)$ gray

1 → ⊕ → 1 ⊕ 0 ⊕ 0

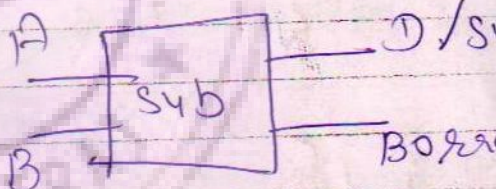
(1 0 1 0) gray

# Gray to Binary

(1100)g



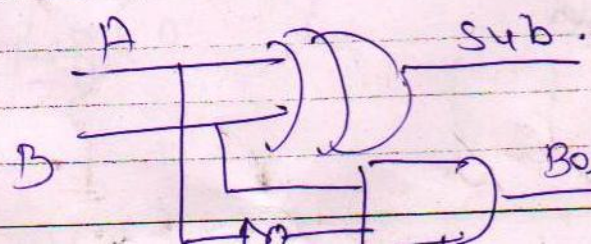

| A | B | S | B |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |




$$S = \bar{A}B + A\bar{B}$$

$$= A \oplus B$$

$$B = \bar{A}B$$



# flip-flop

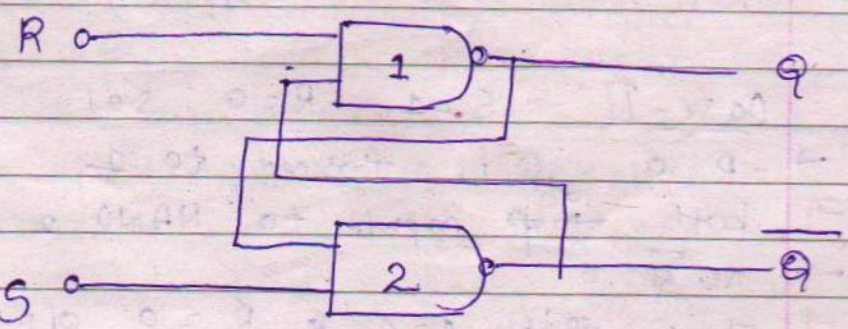
flip-flop is bistable logic ckt i.e its output have two stable states It is a sequential circuit

→ A bistable multivibrator has two stable states. It needs external trigger input to change existing state.

## Types of Flip-Flops :-

1. S-R flip-Flops
2. J-k flip-Flops
3. D flip-flops
4. T flip flops.

## 1 S-R Flip-Flops :-



| S | R | $Q_{n+1}$ | $\bar{Q}_{n+1}$ | |
|---|---|---|---|---|
| 0 | 0 | RACE | RACE | |
| 0 | 1 | 0 | 1 | → Reset |
| 1 | 0 | 1 | 0 | → Set |
| 1 | 1 | NC | NC | → Inactive |

Case-1 S=0, R=0 : Race

→ when any input of a NAND gate becomes 0, its output is forced to 1.

→ This is an undetermined state and hence should be avoided. so also called as Race condition.

Case-II : S=0, R=1 : Reset

→ S=0, it forces Q to be 1

→ Hence both inputs to NAND-1 are 1

→ so Q=0

→ Thus with S=0 & R=1 the outputs are Q=0 & $\bar{Q}$=1

→ This is reset condition

Case-III S=1, R=0 : set

→ R=0, Q is forced to 1

→ both ~~inp~~ inputs to NAND-2 are 1

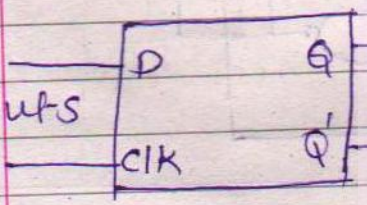
→ so $\bar{Q}$=0

→ Thus with S=1 & R=0 o/p are Q=1 & $\bar{Q}$=0 & This is set condition

Case IV :- S=1, R=1 : No change.

$Q_{n+1}$ = ? There is no change in outputs if S=R=1.

(2) D - flip-flop :-




| D | Q(before) | Q(after) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

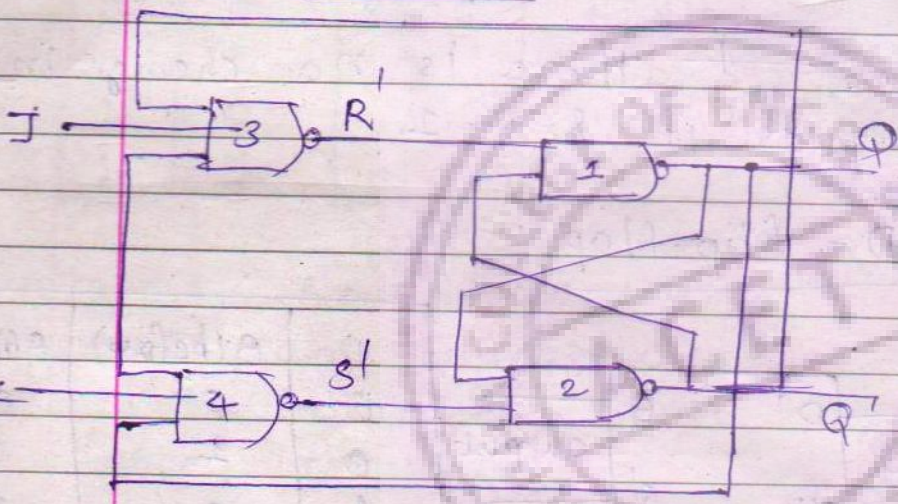
→ If D=0 then Q=0 ; if D=1 then Q=1

→ Therefore we can use the D FF as a latch element.

→ There is a delay called propagation Delay between Q o/p & D input it means if CLK is active, the Q out-put follows D input after some delay Hence D flip-flop can also be used as a delay element in order to introduce a specific amount of time delay.

Application :- 1) As a Delay element
2) In Digital Latches

(3) J-K flip-flop :-




| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| J | K | Clk | $Q_{n+1}$ | $\bar{Q}_{n+1}$ | |
| 0 | 0 | ↑ | $Q_n$ | $\bar{Q}_n$ | N C |
| 0 | 1 | ↑ | 0 | 1 | Reset |
| 1 | 0 | ↑ | 1 | 0 | Set |
| 1 | 1 | ↑ | $\bar{Q}_n$ | $Q_n$ | togg te |

→ output Q is fedback to K input & output $\bar{Q}$ is fedback to J input as shown.

→ with positive clock edge J=0, K=0, the output won't change their previous state

→ If J=0 & K=1 and positive clock edge applied, the Q output becomes 0 & $\bar{Q}$

output 1 this is called Reset condition of JKFF

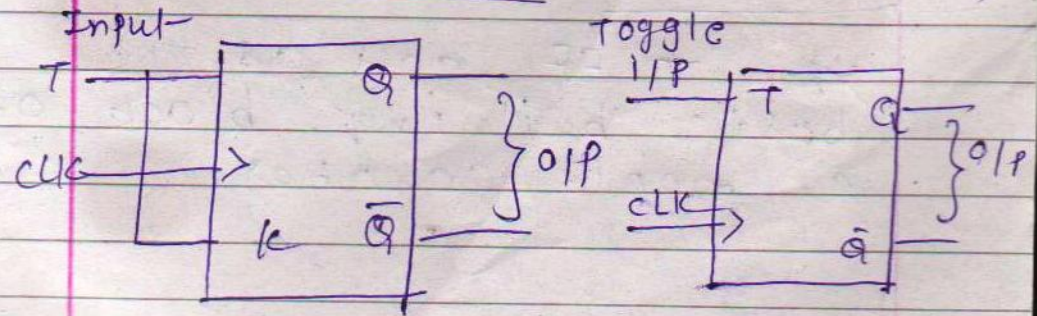
→ If J=1 & k=0 & positive clock edge applied, the Q output becomes 1 & $\bar{Q}$ = 0 this is set condition

→ If J=k=1 & short positive block edge applied the Q output & $\bar{Q}$ output will change to their complements means if Q $\bar{Q}$ = 01 originally then they will change to 1 0 after toggling. this is called as toggle condition of JKFF

## Application :

1 Shift Register
2 Counters

## 4) T- flip-flop (Toggle flip-flop)



| Inputs | | Outputs | | State |
|---|---|---|---|---|
| clk | T | $Q_{n+1}$ | $Q'_{n+1}$ | |
| 0 | X | $Q_n$ | $\bar{Q}_n$ | No change |
| ↑ | 1 | $\bar{Q}_n$ | $Q_n$ | Toggle |

→ Toggle flip-flop is basically a J-K flip-flop with J & K terminals permenantly connected together. It has only one input denoted by 'T'.

→ When T=0, J=k=0. Hence output Q and $\bar{Q}$ will not change even after application of a clock pulse

→ But if T=1 then J=k=1 and outputs will toggle corresponding to every leading edge of clock signal

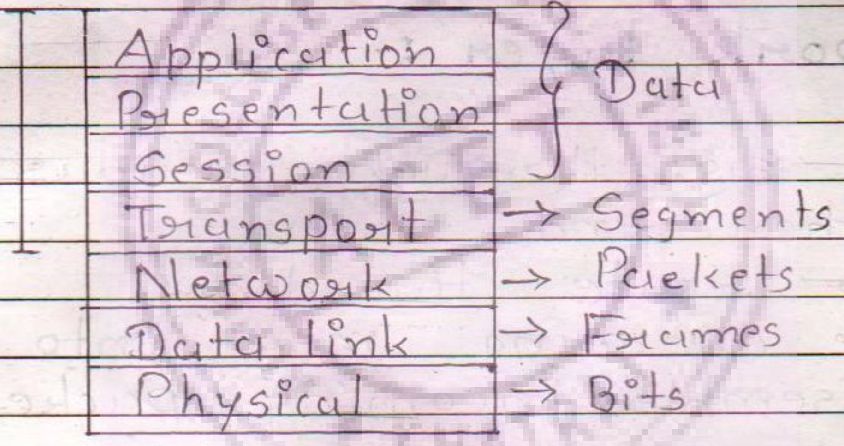
## Application

The T FF acts as the basic building block of a ripple counter

# OSI Reference Model

OSI → Open Systems Inter Connection
Basic Reference Model

- It divides n/w architecture into 7 layers
- From top to bottom.




- It defines seven levels in complete communication system.

## [1] Physical layer :-

- To activate maintain & deactivate the physical connection.
- To define voltage and data rates needed for transmission.
- To convert data bits into electrical sig.
- Simplex or duplex.
- It does not detect error
- & medium or modulation.

## [2] Data link :-

- For synchronization & error control
- It adds error detection bits.
- Encode data.
- Msg is in Frame form & system wait for acknowledgements.

## [3] Network layer :-

- Route sig. through various channels to other end.
- Decide route for data.
- Divide outgoing msg into packets & assemble incoming packets.

## [4] Transport layer :-

- It decide data transmission should take place on parallel or single path.
- It does multiplexing, splitting or segmenting.
- Breaks data groups into smaller units

## [5] Session layer :-

- Manages & synchronizes conversations between two different applications.
- It controls logging on and off user identification, billing & session management

- Data are marked and resynchronized properly.

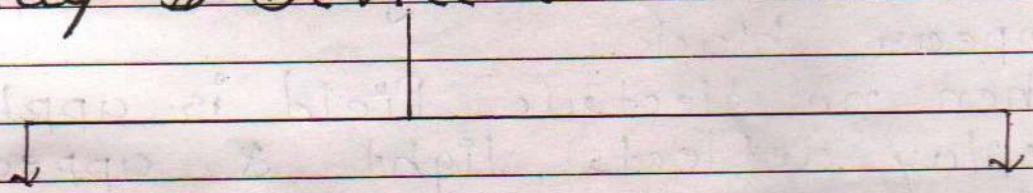
## [6] Presentation layer :-

- It makes sure that the into is in proper form.
- IF both comm. system is diff. (ex. ASCII & IBM's EBCDIC) then this layer provides the translation from ASCII to EBCDIC & vice versa.

## [7] Application layer :-

- At the top
- It provides diff. services ~~retransferring~~ the files of info, distributing the results etc.
- It do login or password checking.

## # Display & Device :-



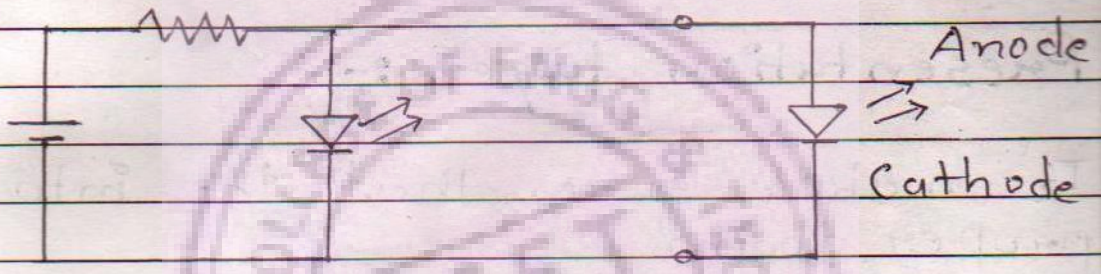
Active devices

- LED

Passive devices

- LCD

## [1] LED (light Emitting Diodes)

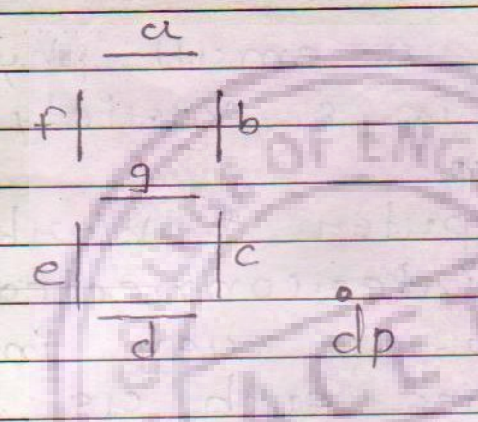



- LED emits light when electrical energy is applied to it.
- two terminal device.
  Anode (A) & Cathod (K)
- basically PN Junction diode
- Available in red, yellow & green colours
- LED req. 10 mA current flow.

## [2] LCD (Liquid Crystal Display)

- It needs very small power (milliwatts)
- IF we apply electric field, the molecules of liquid crystal material are aligned so as to absorb light & display will appear black.
- When no electric field is applied the display reflects light & appears like silver mirror.

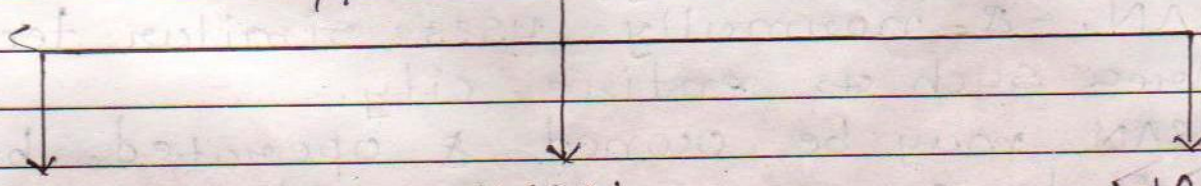
## Seven Segment LED :-




- Most commonaly used numeric display
- 10 - segment & 16 - segment display are used.
- We can display no 0-9.
- It has two types.

1) Common Anode
2) Common Cathode

## * Types of Networks



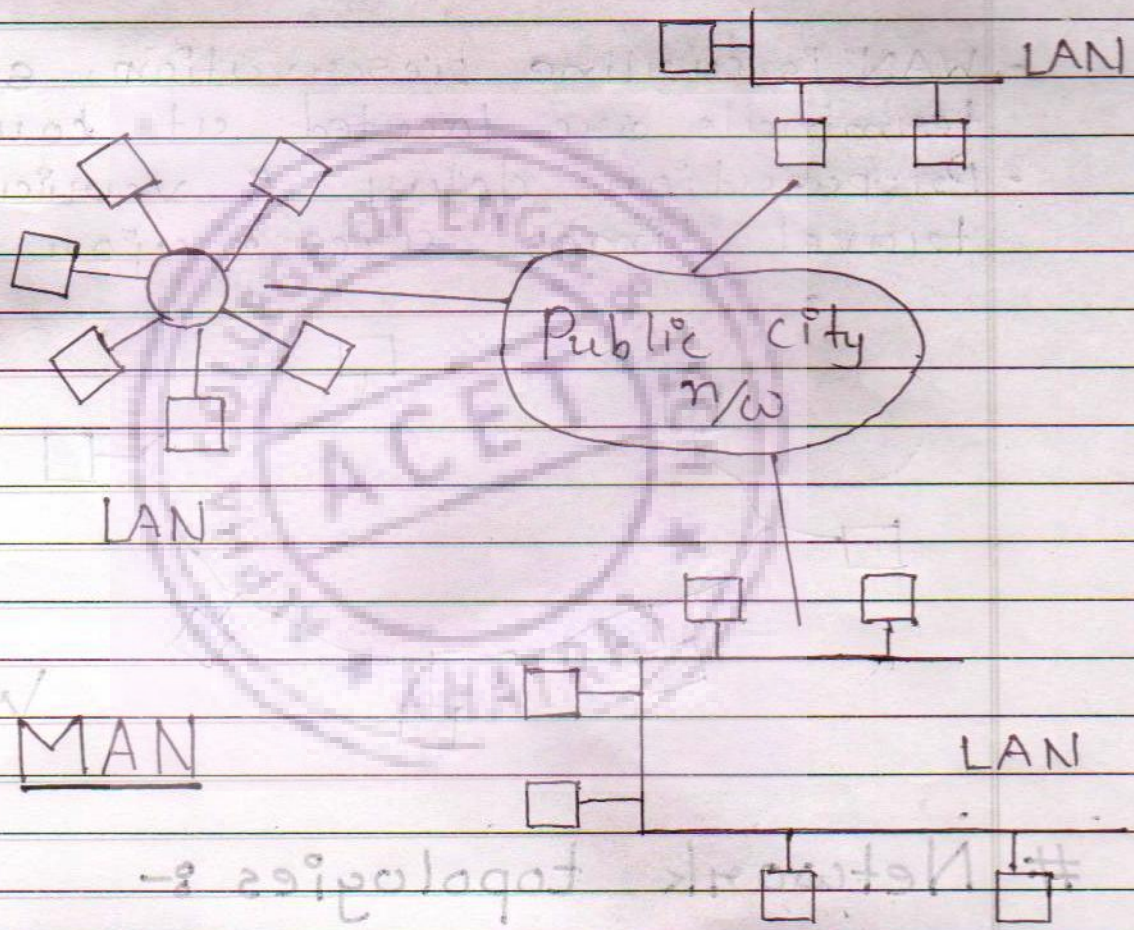

| LAN | MAN | WAN |
|---|---|---|
| local area n/w | Metropolitan area n/w | Wide area n/w |

## [1] LAN :-

- Operate over a small physical area.
- Widely used in a variety of application
- Easy to design
- Personal computer & Work station in offices are interconnected via LAN.
- Info transfer is easy in LAN.
- Diff. topologyies such as Bus, Ring, Star, tree etc.
- Upto few kilometers in size.
- In LAN, one of the computer becomes server serving all remaining computers called clients
- Data rate - 10 Mbps to 1 Gbps
- Bus & Ring topology.

## [2] MAN (Metropolitan Area Network)

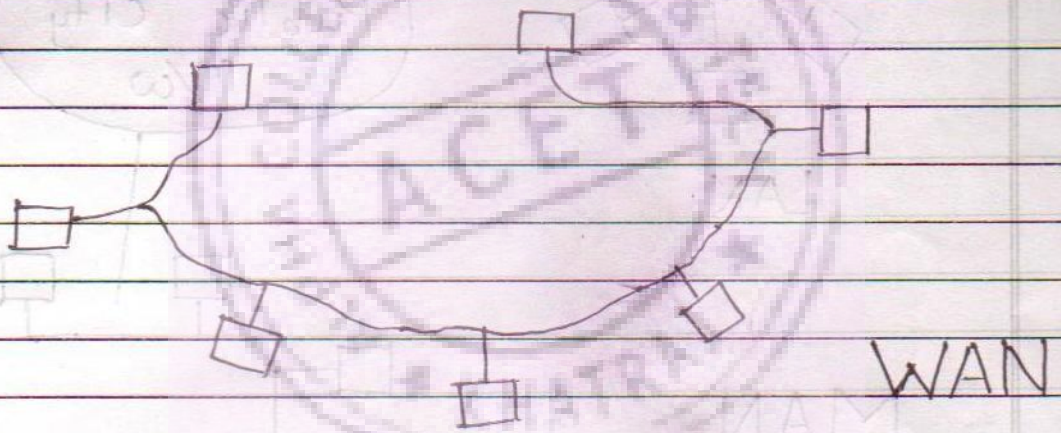
- ~~Man is~~ MAN is bigger version of a LAN, & normally uses similar technology
- Area such as entire city.
- MAN may be owned & operated by private company or by public company. Such as telephone company




## [3] WAN (Wide Area n/w)

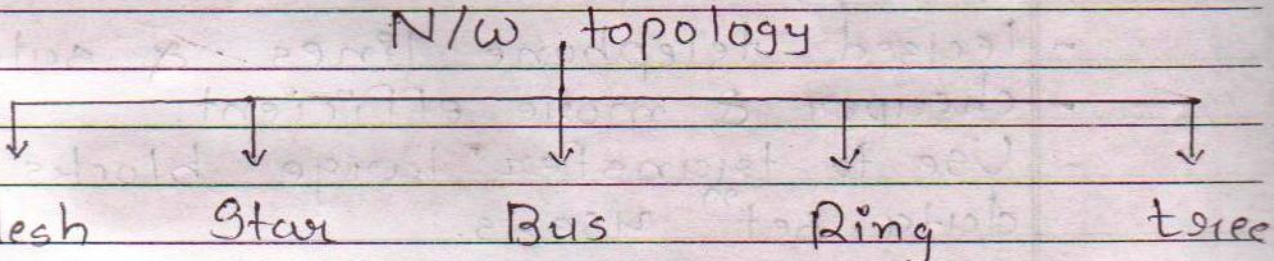
- large distance or when computers to be connected to each other are at widely separated location. then WAN is used.
- leased telephone lines & satellite links.
- cheaper & more efficient.
- Use to transfer large blocks of data betⁿ users.

- WAN is airline reservation system terminals are located at country.
- Propagation delay & variable signal travel times are major problems



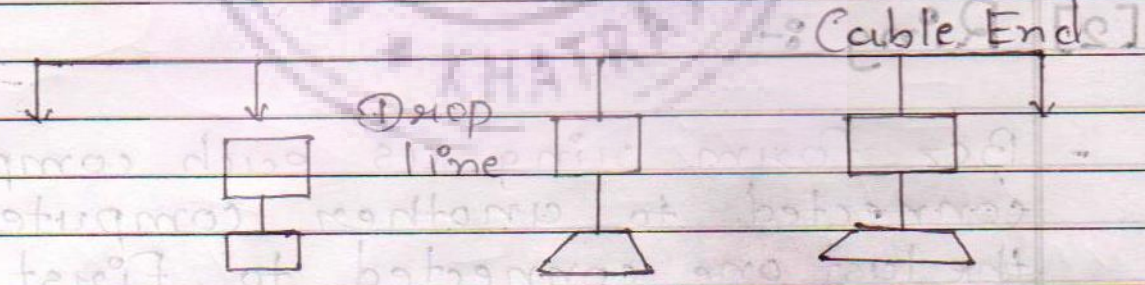

# Network topologies :-

- Devices or nodes in a n/w is connected to each other via comm. link.
- The geometric representation of such a relationship of links & nodes is known as the topology of the n/w



## [1] Bus topology :-

- For small, simple or temporary n/w
- passive topology bcz no amplification simple cable
- Simply destination computer matches add. & get msg.




- transmits data only in one direction
- Every device is connected to single cable.

### Advantage :-

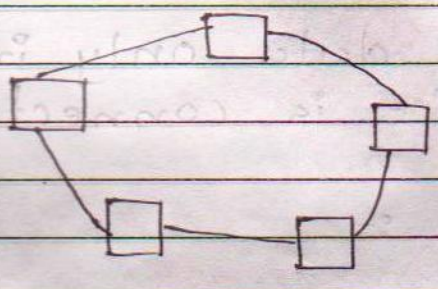
- cost effective
- least cable req. compare to other n/w.
- Use for small n/w
- Easy to understand.
- Easy to connect cable.

Disadvantage :-

- if cable fails whole n/w fails.
- For heavy traffic performance of n/w decreses.
- Cable has limited length.
- Slow then ring topology.

## [2] Ring :-

- Bcz form ring as each computer is connected to another computer with the last one connected to first



- no. of repeaters are used & unidirectional.
- Data transfer sequential.

Advantage :-

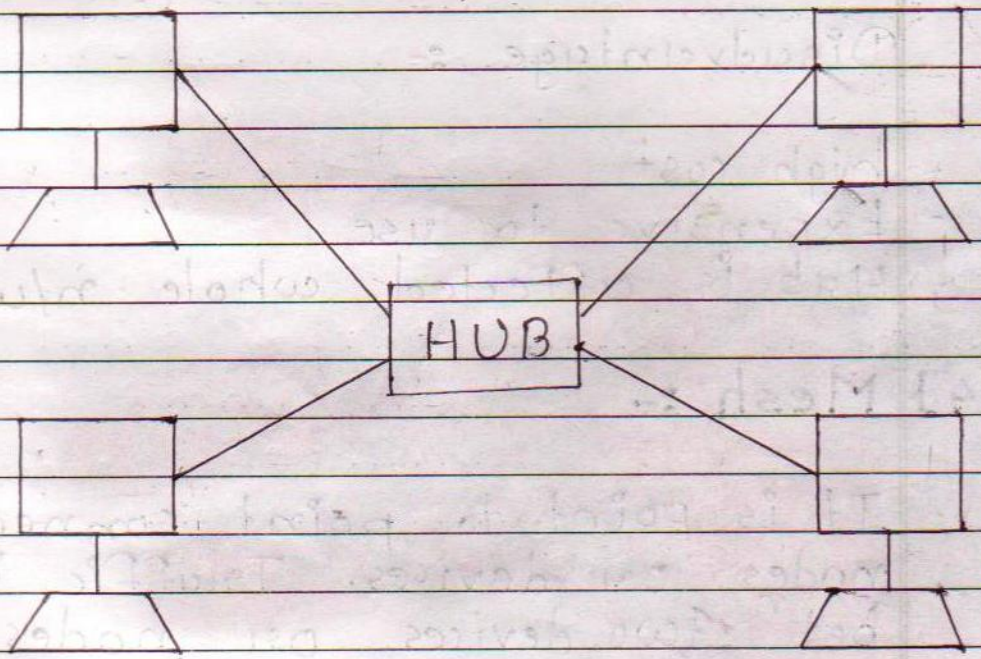
- n/w is not affected by high traffic.
- cheap to install and expand.

Disadvantage :-

- Troubleshooting is difficult.
- Adding or deleting computer disturbs n/w.
- Failure of one computer disturbs the whole n/w.

[3] Star :-

- All the computers are connected to a single hub through cable. This hub is the central node & all other nodes are connected to central node.



- Every node has its own dedicated connection to hub.
- Acts as repeater for data flow
- can be used with twisted pair, optical fibre or coaxial cable.

Advantages :-

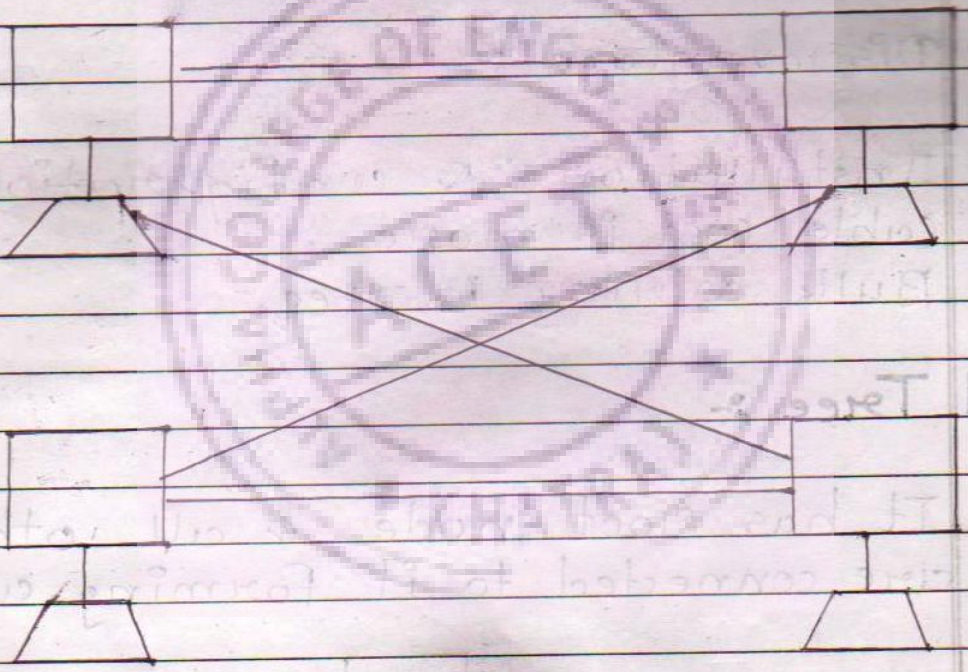
- Fast performance
- Hub can upgraded easily
- Easy to troubleshoot
- Easy to setup & modify
- Only affected node failed rest of node coork smoothly

Disadvantage :-

- high cost
- Expensive to use
- Hub is affected whole n/w stopped.

[4] Mesh :-

- It is point to point connection to other nodes or devices. Traffic is carried only bet$^{n}$ two devices or nodes.



- Mesh has $\left(\frac{n-2}{2}\right)$ physical channels.
- Fully connected
- Robust
- Not flexible

Advantage :-

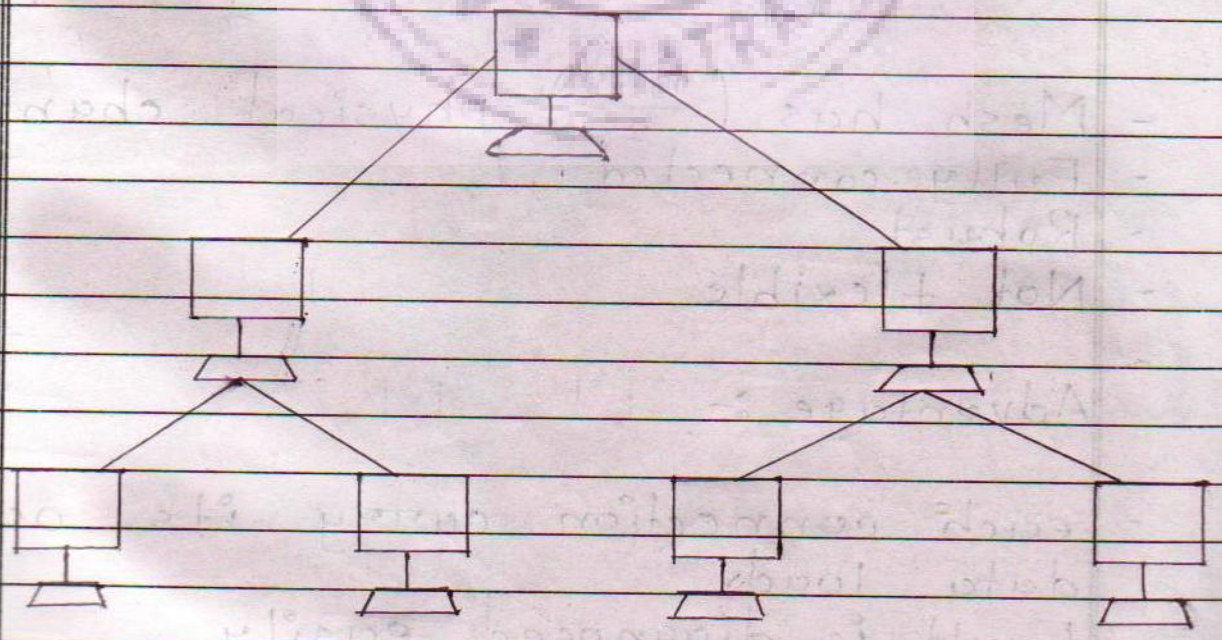
- each connection carry its own data load.
- Fault is diagnosed easily
- provides security & privacy.

Disadvantage :-

- Installation & configuration is difficult
- Cable cost is more.
- Bulk wiring is req.

## [5] Tree :-

- It has root node & all other nodes are connected to it forming a hierachy.

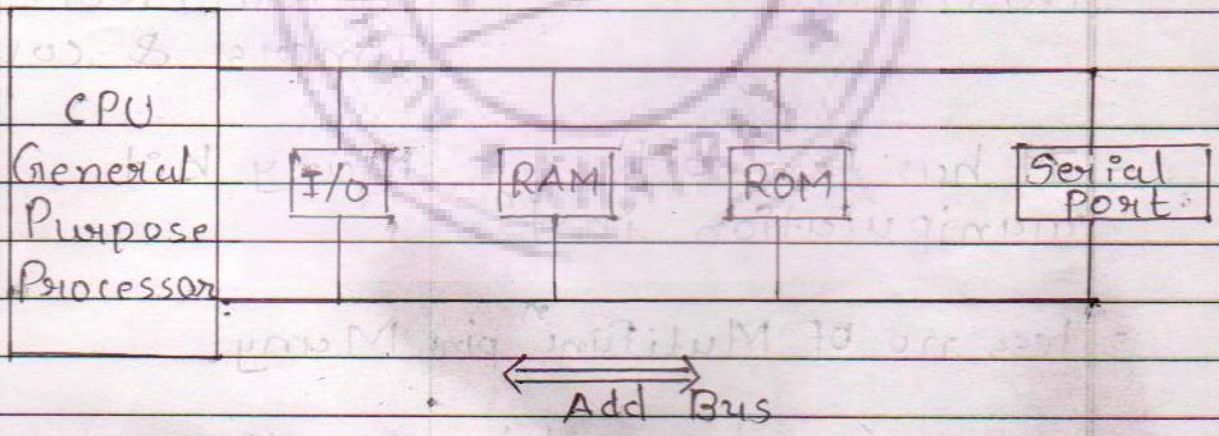


- Used in WAN
- Extension of bus & star topologies.
- Expansion of nodes is possible & easy
- Easily managed & maintained.
- Error detection is easily done

Disadvantage :-

- Heavily cubled
- Costly
- If more node are added maintenance is difficult

## * Microprocessor :-



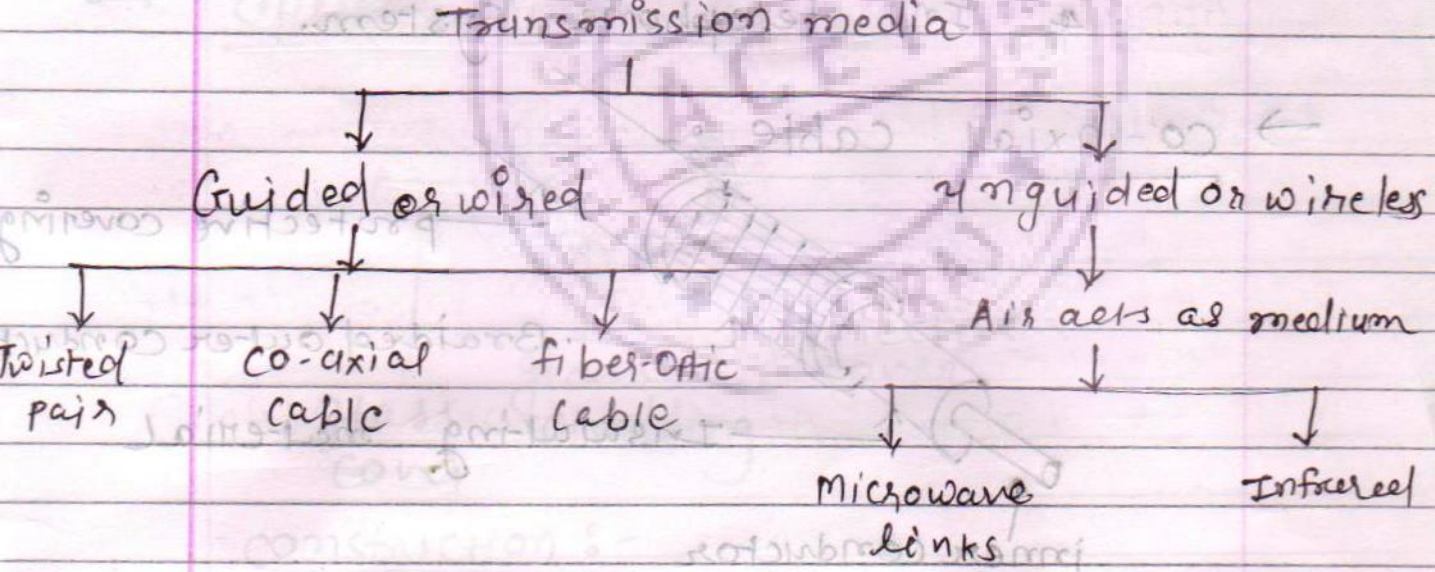

## * Micro Controller

| CPU | RAM | ROM |
|---|---|---|
| I/O<br>---<br>ADC | Timer | Serial<br>COM<br>Port |

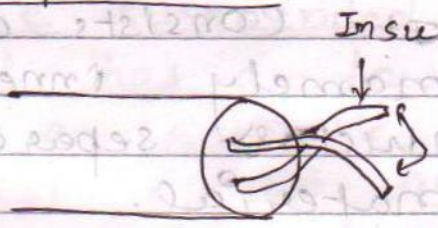
| | μP | μC |
|---|---|---|
| - | μP is chip that dependent on the chip of many functions. | μc is single chip micro computer that has everything in-built. |
| - | A mp contain ALU register & control circuit. | A contains the circuitry of MP & has built in RAM, ROM, I/O Timers & counter. |
| - | It has few bit manipulation inst$^{n}$ | Many bit |
| - | less no of Mutifunc$^{n}$ pins | Many |
| - | Large memory add space. | Small |
| - | Design is flexible. | less flexible |
| - | req. more Hardware | less |
| - | High Power Consumption | low |
| | 8085, 8086 | 8051, AVR |

☆ What is transmission medium? what are the different types of transmission medium?

Ans Media are what the message is transmitted over. In other word a communication channel is also called as a medium.




Twisted pair cables:-




→ two type of twisted pairs:-
1) Unshielded twisted pair
2) ~~Twisted~~ shielded twisted pair

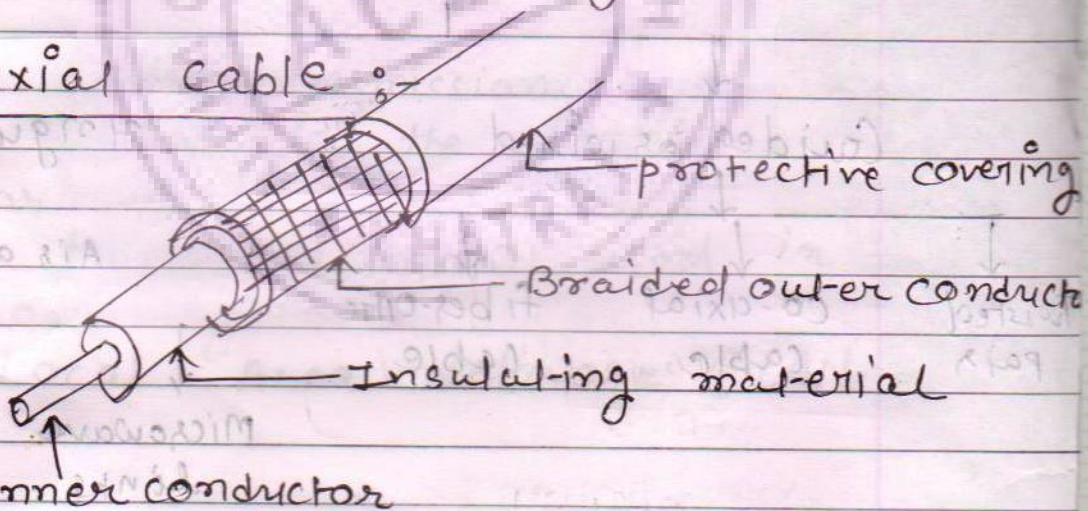
UTP:- A twisted pair consists of two insulated conductor twisted together in shape of spiral

STP:- has a metal foil or braided mesh included in order to cover each pair of twisted insulating conductors

App^n.

1. LAN for connecting computer to each other
2. In ISDN
3. In DSL
4. In telephone System.

→ Co-axial cable :-




The construction of co-axial cable is as shown. It consists of two conductors namely inner & a outer conductor separated by dielectric material.

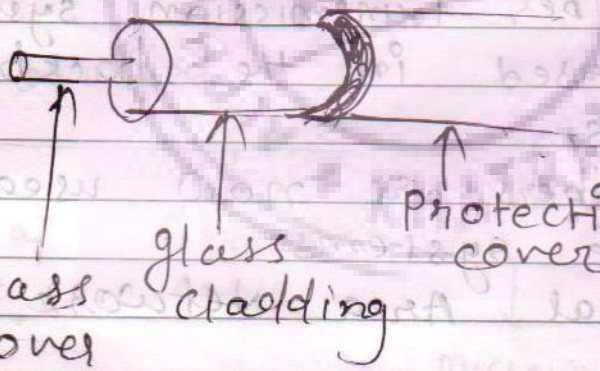
Characteristics :-

→ It has a large bandwidth & low losses
→ easy to install
→ relatively inexpensive

## Applications :-

1) Analog telephone networks
2) Digital telephone networks
3) Cable TV
4) Digital transmission
5) Fast Ethernet.

→ ## optical fiber cable :-




### construction :-

It consists of an inner glass core surrounded by glass cladding which has a lower refractive index and a protective covering

→ Digital signals are transmitted in the form of intensity - modulated light signal which is trapped in glass core

### Advantages :

→ small size & light weight
→ Easy availability & low cost

3) No electrical interference
4) Large bandwidth

Disadvantages :-

1) The initial cost is high
2) joining optical fibers is difficult job

Applications :-

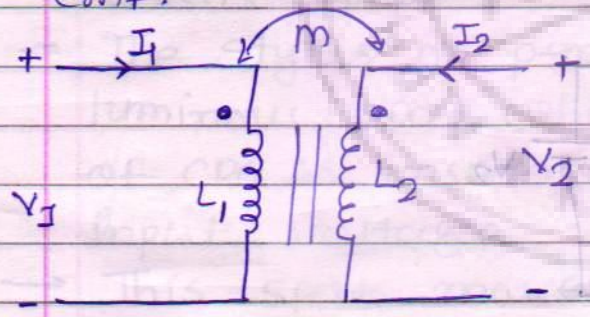
1) optical fiber transmission system are widely used in the backbone of networks.
2. optical fibers are now used in the telephone systems
3. In Local Area Network (LANs)

* Dot Convention :-

→ The two coils used in the mutual inductance experiment can be modelled as show in fig. which shows the two coil system.

→ In fig $L_1$ and $L_2$ represent the self inductance of the two coil and M is the mutual inductance between them.

→ The two dot points marked on the two coils help us to determine the polarity of the mutually induced emf with respect to the self inducted emf.




* Rules of dot convention :-

Rule 1 :- If current enters into the dots of both the coil or comes out of the dots of both the coils, then the mutually induced voltages add to the self induced emfs for both the coils because the self and mutually induced emfs have the same polarities.

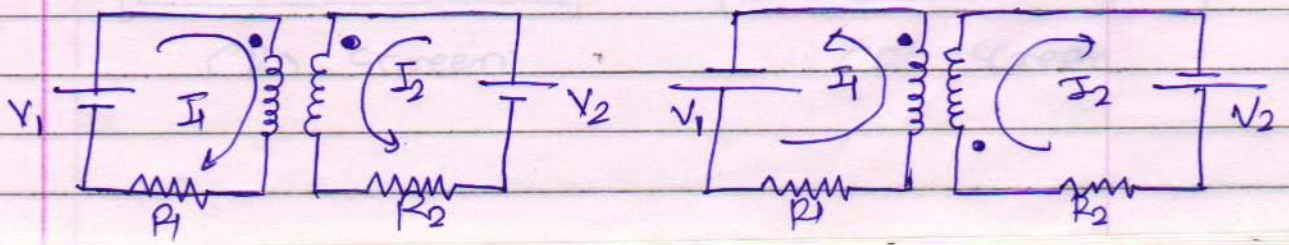


Illustration of Rule 1:

$$V_1 = I_1 R_1 + L_1 \frac{dI_1}{dt} + M \frac{dI_2}{dt}$$

$$V_2 = I_2 R_2 + L_2 \frac{dI_2}{dt} + M \frac{dI_1}{dt}$$

Rule 2: If current enters into the do in one coil and comes out of the dot in the other coil, then the self induce emfs and the mutually induced emfs co have opposite polarities with respect to each other.

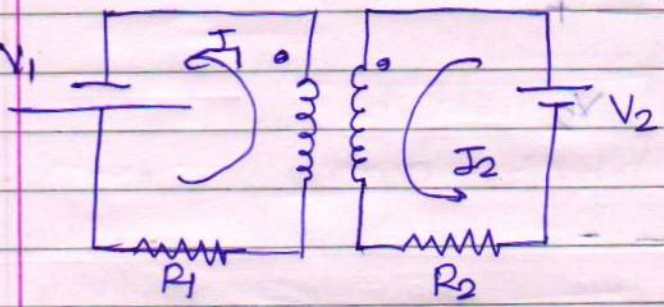



Illustration of rule 2

$$V_1 = I_1 R_1 + L_1 \frac{dI_1}{dt} - M \frac{dI_2}{dt}$$

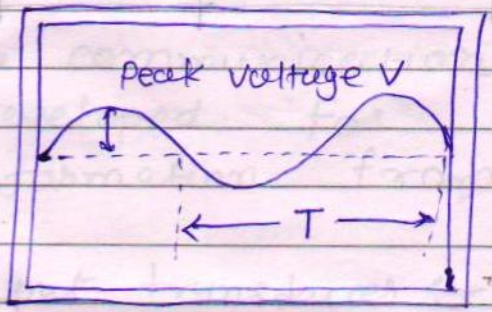
$$V_2 = I_2 R_2 + L_2 \frac{dI_2}{dt} - M \frac{dI_1}{dt}$$

* write short note on CRO.

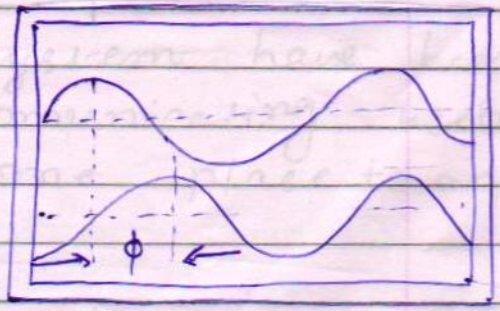
→ The cathode Ray Oscilloscope (CRO) is a very useful electronic instrument which is used in college laboratories and industries for measurement of voltage, time, freq, phase shift and for observing the shape of input waveform.

- Thus we can call the CRO as a very fast X-Y plotter which moves & displays an input signal versus another signal or versus time.
- The stylus or pen of this X-Y plotter is a luminous spot which moves over the screen of CRO in response to the changes in the input voltage.

→ This spot moves very rapidly on the screen. So due to persistence of vision, we feel that a continuous waveform is being displayed.




CRO Screen




CRO Screen

## ✱ comparison between DSB-FC, DSB-SC, SSB and VSB.

| Sr No. | parameter | DSB-FC | DSB-SC | SSB | VSB |
|---|---|---|---|---|---|
| 1 | carrier suppression | NA | fully | Fully | N.A |
| 2. | sideband suppression | N.A | N.A | one S.B completely | one S suppressed partia |
| 3 | Bandwidth | $2f_m$ | $2f_m$ | $f_m$ | $f_m < BW <$ |
| 4 | Transmission efficiency | Minimum | moderate | max | moderat |
| 5 | No. of modulating inputs | 1 | 1 | 1 | 2 |
| 6 | Application | Radio broadcasting | Radio Broadcasting | Point to point mob communication | T. V |
| 7 | power requirement to cover same area | High | medium | very small | modera |
| 8 | complexity | simple | simple | complex | simpler than SSB |

Page No.
Date / /

## ★ Comparison between DSB-FC, DSB-SC, SSB and VSB.

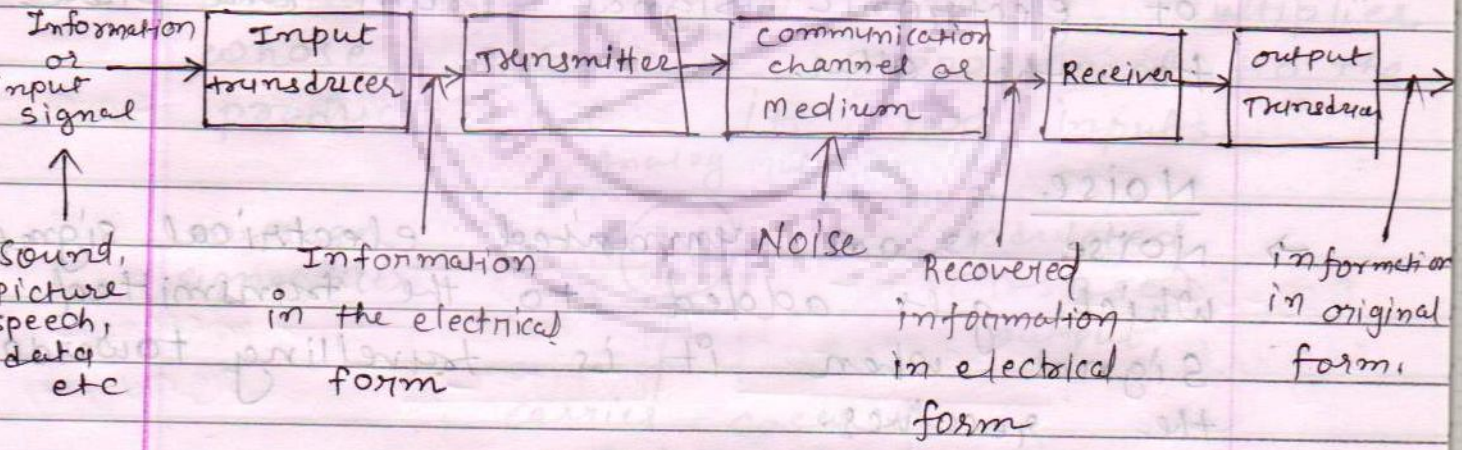
| Sr No. | parameter | DSB-FC | DSB-SC | SSB | VSB |
|---|---|---|---|---|---|
| 1 | Carrier Suppression | NA | fully | fully | N.A |
| 2. | sideband suppression | N.A | N.A | one S.B completely | one S.B suppressed partially |
| 3 | Bandwidth | $2f_m$ | $2f_m$ | $f_m$ | $f_m < BW < 2f_m$ |
| 4 | Transmission efficiency | Minimum | moderate | max | moderate |
| 5 | No. of modulating inputs | 1 | 1 | 1 | 2 |
| 6 | Application | Radio broadcasting | Radio Broadcasting | Point to point mob communication | T.V |
| 7 | power requirement to cover same area | High | Medium | very small | moderate |
| 8 | complexity | simple | simple | complex | simpler than SSB |

# Chapter - 5

Page No.
Date / /

Q-1 Draw & Explain functional block diagram of signal processing system.

Ans The block diagram of the simplest possible communication system is as shown. We can also say that it is block schematic of signal processing system.




## Information or input signal :-

The communication system have been developed for communicating useful information from one place to another

## Input transducer :-

The information in the form of sound, picture or data signals cannot be transmitted as it is.

## Transmitter :-

The function of transmitter block is to convert electrical equivlent of the information to a suitable form.

## communication channel or medium :-

medium is path used for transmission of electronic signal from one place to the other.

## Noise :-

→ Noise is an unwanted electrical signal which gets added to the transmitted signal when it is travelling towards the receiver.

## Receiver :-

The process of reception is exactly opposite process of transmission.

## Output transducers :-

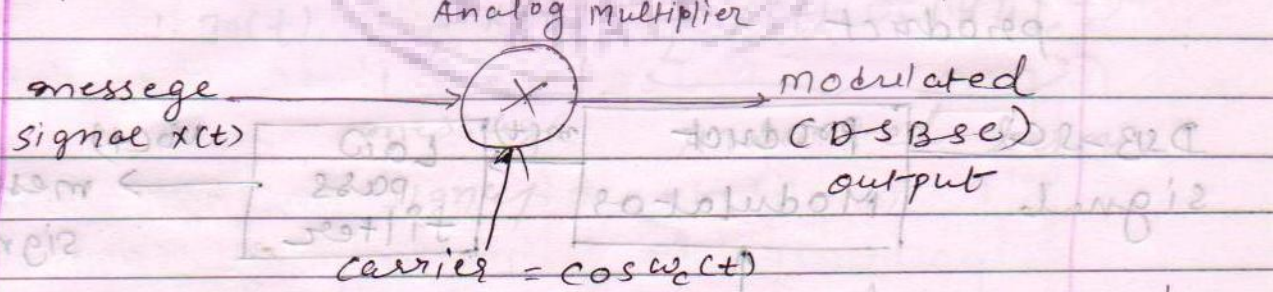
The output transducer converts electrical signal at output of receiver back to the original form i.e sound or TV pictures. etc.

Q. Explain in brief product Modulation and Demodulation with necessary diagrams

Ans product modulator :-

Here modulation is achieved by directly multiplying message signal x(t) by the carrier $\cos\omega_c t$.

→ The multiplication of $x(t)$ & $\cos\omega_c t$ is carried out in an analog multiplier whose output is proportional to the product of its two inputs.




we can prove that- output is DSB-SC signal

Let $x(t) = \sin\omega_m t$

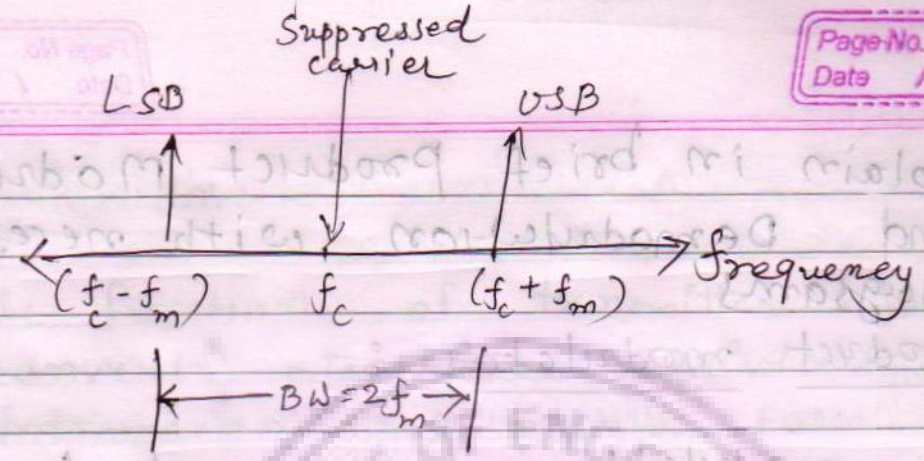
The multiplier output $= x(t)\cos\omega_c t = \sin\omega_m t \cos\omega_c t$

we know that

$2\cos A \sin B = \sin(A+B) - \sin(A-B)$

$\therefore$ multiplier output $= \frac{1}{2}\cos(\omega_c+\omega_m)t - \frac{1}{2}\sin(\omega_c-\omega_m)t$

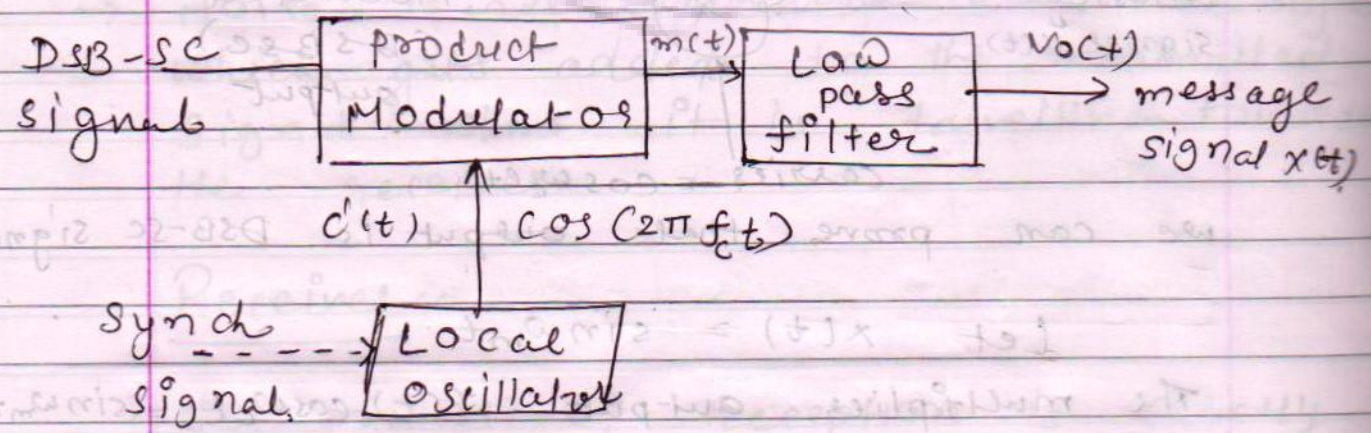
↑ USB ↑ LSB




## Product Demodulator :-

→ In order to recover modulating signal $x(t)$ back from the modulated (DSB-SC) signal,

→ DSB-SC wave $s(t)$ is applied to a product




Let output of Local oscillator be given by

$$c'(t) = \cos(2\pi f_c t)$$

Thus its amplitude is 1, frequency is $f_c$ Hence output of product modulator is given by,

$$\therefore m(t) = s(t) \cdot c'(t)$$

But $s(t)$ = DSB-SC input = $x(t) \cdot \cos(2\pi f_c t)$

& $c'(t)$ = Local carrier = $\cos(2\pi f_c t)$

$$\therefore m(t) = x(t) \cdot \cos(2\pi f_c t) \cos(2\pi f_c t)$$

$$\therefore m(t) = x(t) \cdot \cos^2(2\pi f_c t)$$

$$\cos A \cos B = \frac{1}{2}[\cos(A+B) + \cos(A-B)]$$

$$\therefore \cos^2(2\pi f_c t) = \frac{1}{2}[1 + \cos 2(2\pi f_c t)]$$

$$= \frac{1}{2} + \frac{1}{2}\cos(4\pi f_c t)$$

$$\therefore m(t) = \frac{1}{2}x(t) + \frac{1}{2}x(t)\cos(4\pi f_c t)$$

message signal — unwanted term

Q- Explain pulsmodulation in Detail

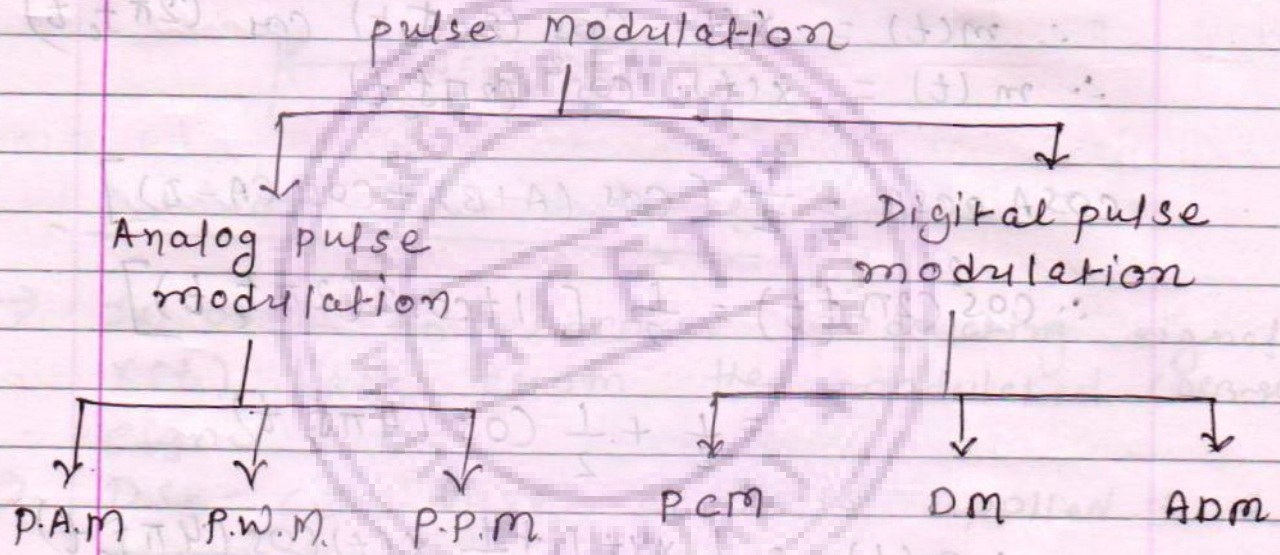
Ans pulse modulation :-

→ In pulse modulation, the carrier is in the form of train of periodic rectangular pulses.

→ Need :- we convert a continuous analog signal in to discrete signal which can be eventually converted

into a digital signal.

→ Type of pulse Modulation :-




① PAM :- (pulse Amplitude Modulation)

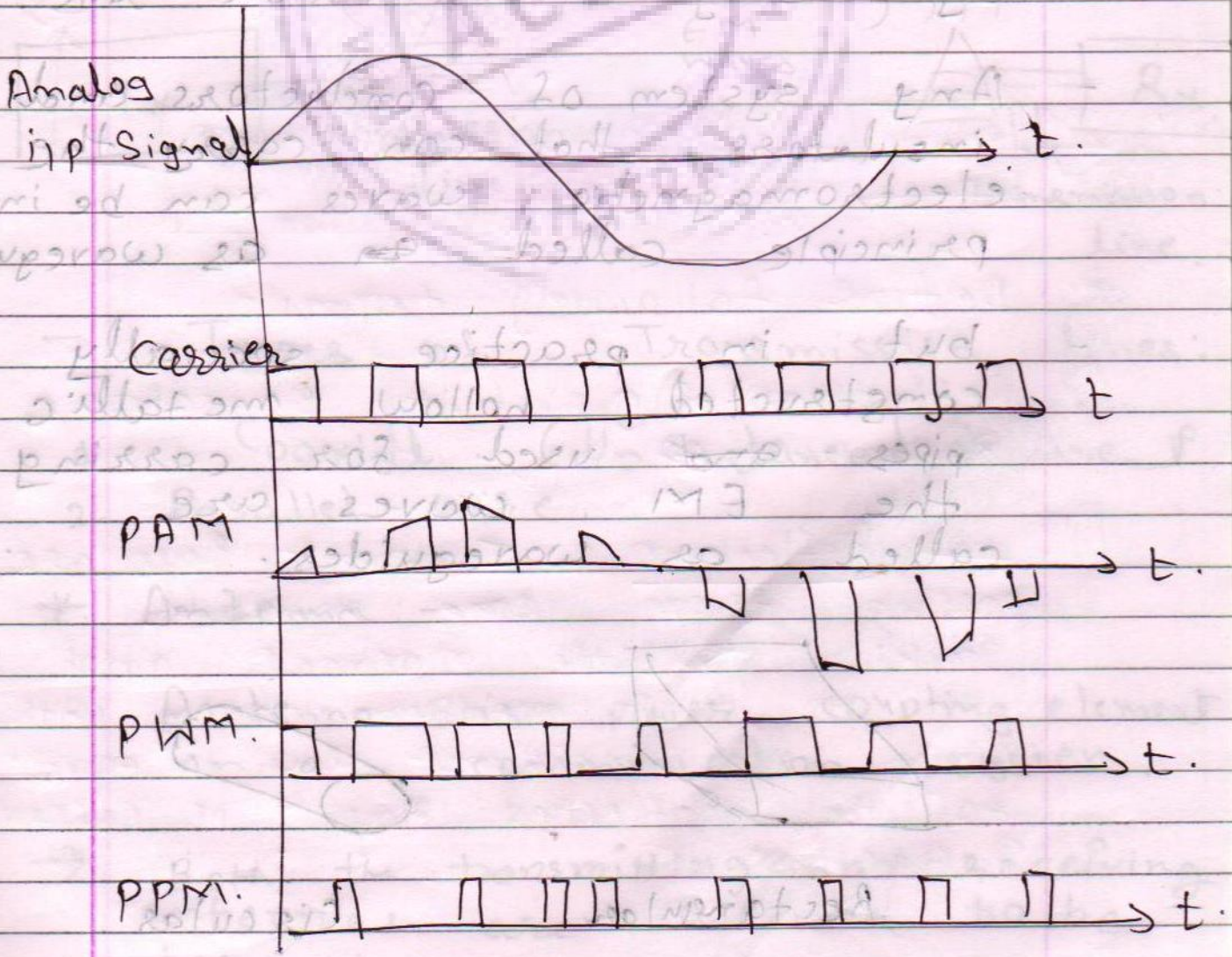
The amplitude of a constant width position is rectangular carrier varied in proportion with instantaneous magnitude of modulating signal

② PWM :- pulse width Modulation :

- Width of carrier pulses is made ~~of~~ to vary in proportion with the instantaneous magnitude of the modulating ~~sing~~ signal

③ PPM. (Pulse Position Modulation)

- the amplitude & and width of the pulses is kept constant. but the position of each pulse is varied in accordance with amplitudes



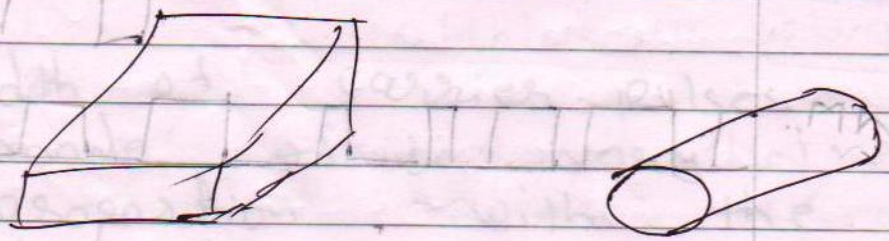
* Define Wave guide, Transmission lines and Antenna.

→ Wave guide:-

It is possible to guide radio waves from one point to the other in an enclosed system by using transmission line.

- Any system of conductors and insulators that can carry the electromagnetic waves can be in principle called as waveguide

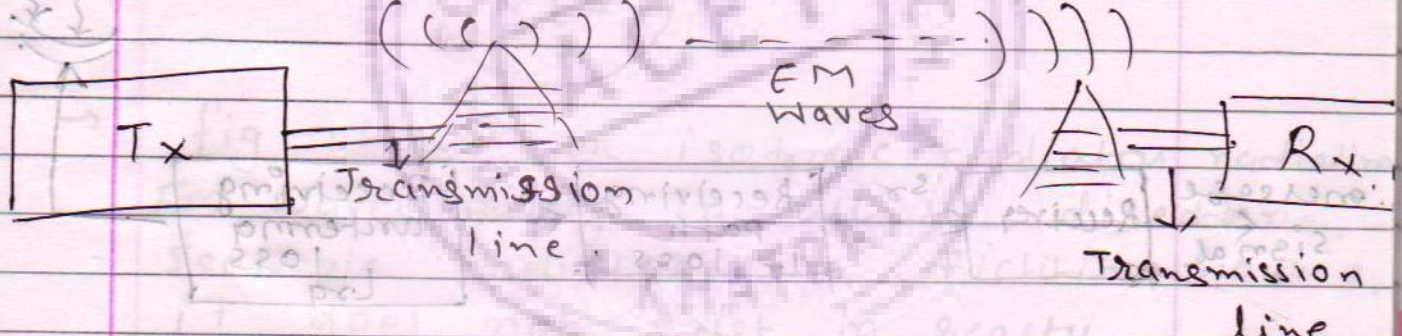
- but in practice specially constructed hollow metallic pipes used for carring the EM waves are called as waveguides.



Rectangular Circular.

- Transmission lines :-

- the electrical signal take from the transmitter output to the transmitting antenna by speeial conductor called transmission lines.



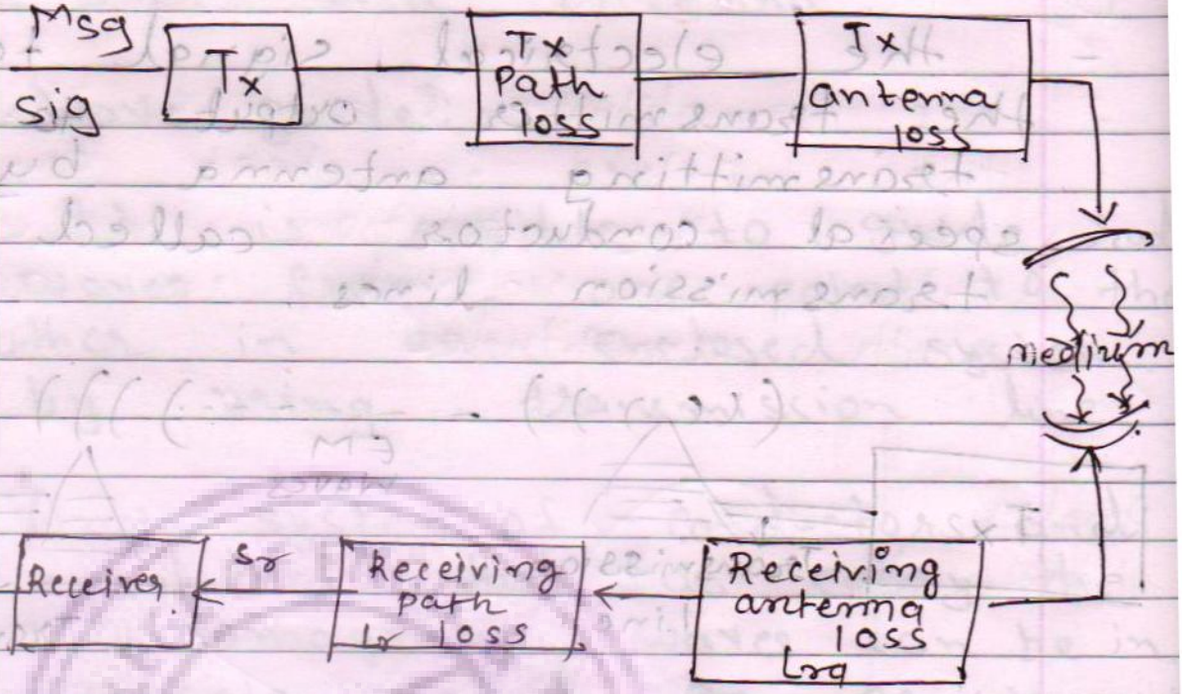

- Types of Transmission lines:

1 Coaxial (Un balanced) line &
2 Parallel - wire.

* Antenna :-

- Antenna is power coupling element in a communication system.

→ Both the transmitting and receiving antennas are assumed to be lossless



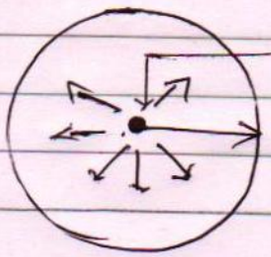

* Define following terms:-

1) Reflection 2) Directivity 3) isotropic Radiator

1) Reflection :- Incident Rays are passing from one medium, Strikes to the normal and go to that medium only with angle of incident Ray is equal to the Reflected Ray. is called Reflection.

## Isotropic Radiator :-

→ An. isotropic radiator is a point source antenna which radiates equally in all the directions.




→ fig shows an isotropic radiator radiating Em waves equally in all the directions. Isotropic radiator is a fictitious source. it does not exist in realty.

## Directivity :-

The Directive gain can be defined in any direction. However directivity means maximum directive gain which is obtained in only one direction in which radiation is maximum.

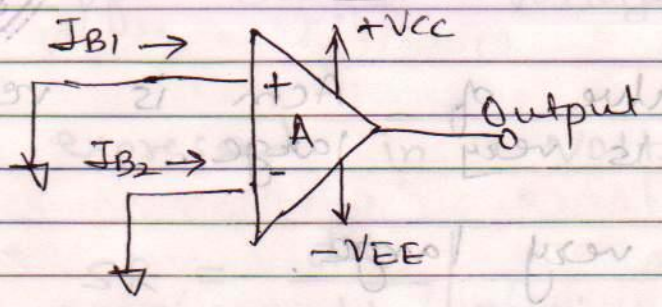
∴ Directivity = Maximum directive gain

OP-1 Q. Explain in brief following properties of operational Amplifier. 1. Input Resistance 2. Open loop voltage gain 3. CMRR 4.

1. Input offset voltage :

- When no input is applied to op-Amp, output voltage should be zero.
- But practically, due to differential input stage, we observe some output voltage.
- Input offset voltage is the voltage that must be applied between two input terminals of op-amp to null the output.
- It is denoted by Vio.
- Vio is normally in mV and Ideal it should be zero.
- For IC 741 max. value of Vio is 6 mV d

2. Input offset current :






- It is denoted by Iio.
- Iio is algebric difference between the currents into inv. and non-inv. terminals of op-amp.

$$I_{io} = |I_{B_1} - I_{B_2}|$$

- Value of Iio for IC 741 is 200nA.

3. Input Bias Current :

It is denoted by $I_B$

$I_B$ is the average of the currents that flow into inverting & non-inv i/p terminals of op-amp.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

For IC 741 value of $I_B$ is 500 nA.

4. Common Mode Rejection Ratio (CMRR) :

It is define as the ratio of differential voltage gain($A_d$) to the common-mode voltage gain($A_{cm}$).

$$CMRR = \frac{Ad}{Acm}$$

Generally value of Acm is very small and Ad = A is very large.

∴ CMRR is very large.

5. Supply voltage rejection ratio (SVRR) :

The change in an op-amp's input offset voltage ($V_{io}$) caused by variation in supply voltages is called SVRR.

→ SVRR is also called as PSRR i.e Power Supply rejection ratio

→ and Power Supply sensitivity (PSS).

$$PSRR = \frac{\Delta V_{io}}{\Delta V}$$

where $\Delta V_{io}$ – change in input offset voltage.
$\Delta V$ – change in supply voltage

→ For IC 741 its value is 150 μV/V.

→ Practically its value should be as small as possible and Ideally it should be zero.

6. Slew rate (SR):

SR is define as the maximum ~~range~~ rate of change of output voltage per unit of time.

→ It's expressed in volts per micro seconds

$$SR = \left.\frac{dV_o}{dt}\right|_{maximum} \quad V/\mu s.$$

→ for IC 741 its value is 0.5 V/μs.

→ slew rate should be ideally infinity and practically as high as possible.

7. Differential Input resistance ( $R_i$ )

- also called as input resistance is the equivalent resistance that can be measured at either inv. or non-inv input terminal with other terminal connected to ground.
- For IC 741 its value is 2 MΩ
- Practically value of input resistance should be as high as possible and ideally it should be ∞.

8. Output Resistance ( $R_O$ ) :

- $R_O$ is equivalent resistance that can be measured bet$^n$ output terminal of op-amp and ground.
- For IC 741 it is 75 Ω.
- Ideally - 0, practicall - as low as possible

9. Input capacitance ( $C_i$ ) :

- $C_i$ is the equivalent capacitance, measured at either inverting or non-inverting termind with other termind connected to ground.
- For IC 741 value of $C_i$ is 1.4 pF
- Practically ~~it is~~ its value should be smal ideally zero.

10. Large signal voltage gain :

- Voltage gain of amplifier is define as the ratio of output voltage to differential input voltage.

$$A = \frac{V_O}{V_{id}}$$

$V_O$ – O/P vtg.
$V_{id}$ – differential I/P vtg.

- For IC 741 its value is 200,000.

11. Bandwidth of Gain – Bandwidth product :

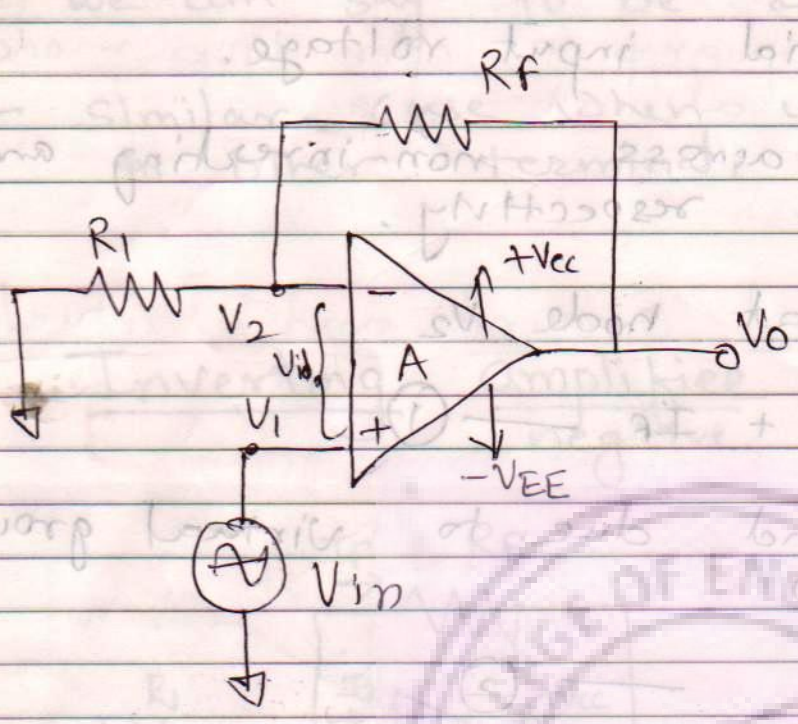
- GB product is the bandwidth of the op-amp when voltage gain is 1.
- For IC 741 its value is approximatly 1 MHz.

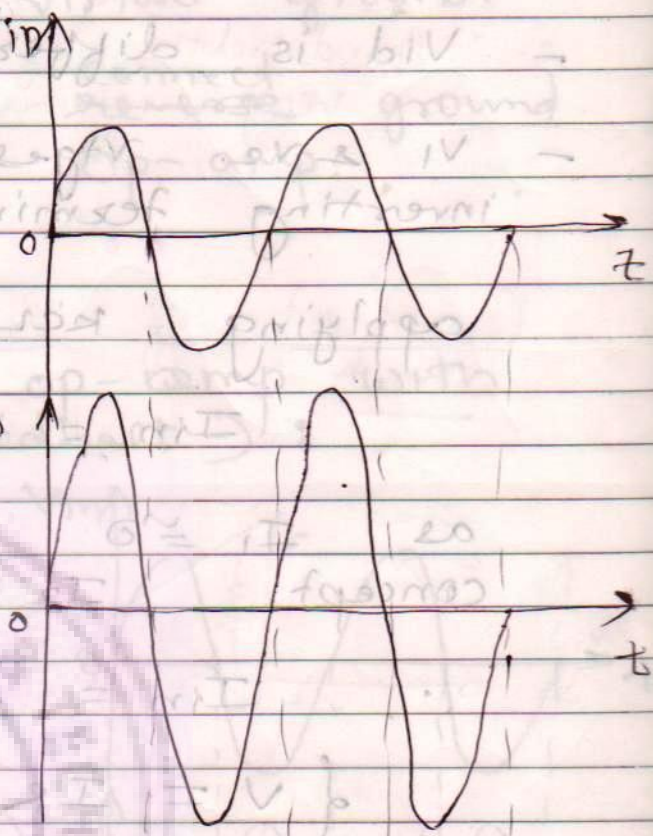
12. Input voltage range :

- When same voltage is applied to both input terminals, the voltage is called common-mode voltage $V_{cm}$.
- For IC 741C $V_{cm}$ applied to both terminal can be ± 13 V.

OP-12 operational amplifier and explain in brief.

## Non-Inverting amplifier (with negative feedback):




- Signal which is to be amplified is applied to the non-inverting terminal of op-amp.
- Rf is feedback resistor.

$$A = \frac{V_o}{V_{id}} \quad \text{---} (1)$$

$$A = \frac{V_o}{(V_1 - V_2)}$$

$$\therefore V_o = A(V_1 - V_2) \quad \text{---} (2)$$

from fig. $V_1 = V_{in}$

& $V_2 = V_o \cdot \frac{R_1}{R_1 + R_f}$

putting this value in eqn (2)

$$V_o = A\left(V_{in} - \frac{V_o \cdot R_1}{R_1 + R_f}\right)$$

$$V_o = AV_{in} - \frac{A \cdot V_o \cdot R_1}{R_1 + R_f}$$

$$V_o + V_o \cdot \frac{A \cdot R_1}{R_1 + R_f} = AV_{in}$$

$$V_o\left(1 + \frac{AR_1}{R_1 + R_f}\right) = A \cdot V_{in}$$

$$V_o\left(\frac{R_1 + R_f + AR_1}{R_1 + R_f}\right) = A \cdot V_{in}$$

$$\therefore V_o = A \cdot V_{in}\left(\frac{R_1 + R_f}{R_1 + R_f + AR_1}\right) \quad \text{---(3)}$$

as $AR_1 >> R_1 + R_f$

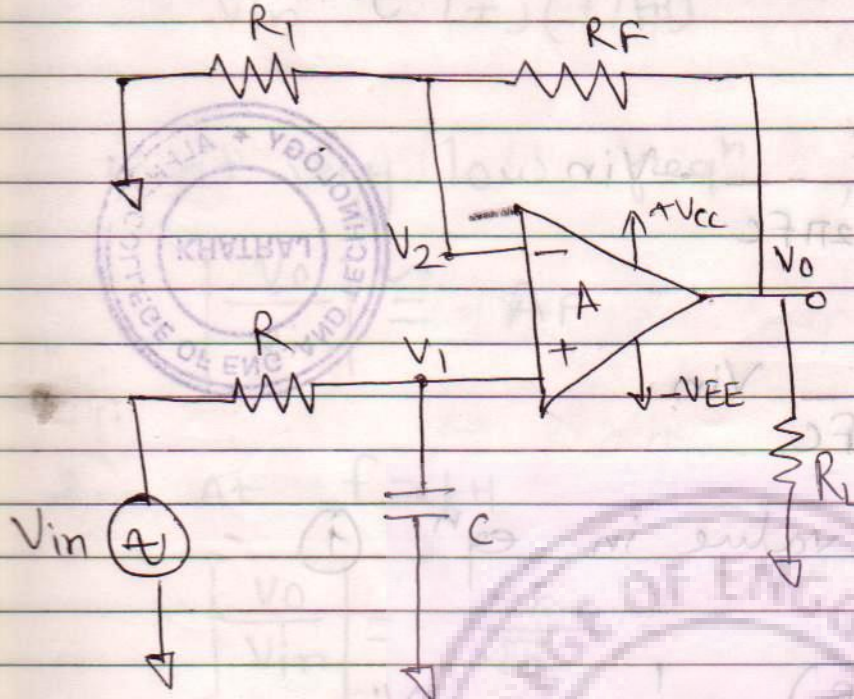
eqn (3) written as

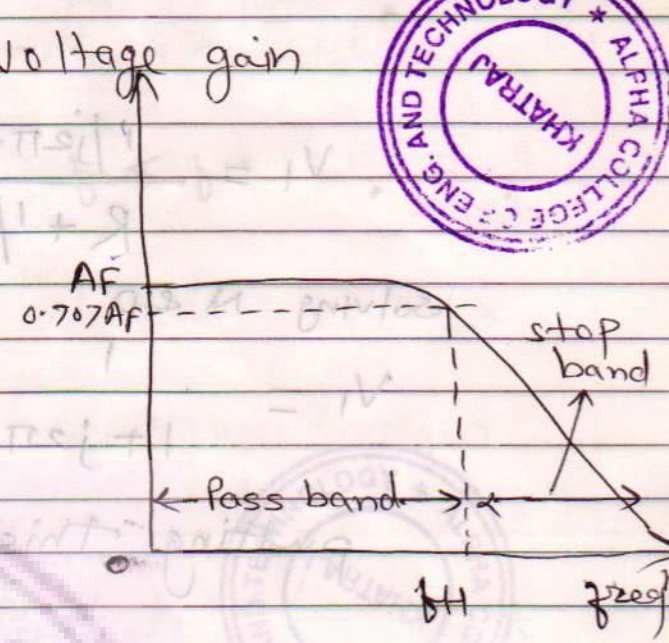
$$V_o = A \cdot V_{in}\left(\frac{R_1 + R_f}{AR_1}\right) = V_{in}\left(1 + \frac{R_f}{R_1}\right)$$

$$\boxed{V_o = V_{in}\left(1 + \frac{R_f}{R_1}\right)}$$

Q. Describe low pass active filter using Op-amp with diagrams & equations.

## Active low pass Butterworth filter :




Frequency Response

- Low pass filter uses RC network for filtering.
- Op-amp is used in non-inverting configuration
- R1 & Rf determines the gain of filter
- Low range of frequencies are passed and higher frequencies are attenuated by this filter as shown in graph.
- output voltage for ampl$^r$ is

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) \cdot V_1 \quad \text{——} (1)$$

Now $$V_1 = \frac{-jX_C}{R - jX_C} \cdot V_{in}$$

where $j = \sqrt{-1}$ & $-jX_C = \frac{1}{j2\pi fC}$

$$\therefore V_1 = \frac{1/j2\pi fC}{R + 1/j2\pi fC} \cdot Vin$$



solving N & D

$$V_1 = \frac{1}{1 + j2\pi RFC} \cdot Vin$$

putting this value in eqn (1)

$$V_0 = \left(1 + \frac{R_f}{R_1}\right) \cdot \frac{1}{1 + j2\pi RFC} \cdot Vin$$

if $f_H = \frac{1}{2\pi RC}$ = higher cutoff freq$^n$ of filter

$$\boxed{V_0 = \left(1 + \frac{R_f}{R_1}\right) \frac{1}{1 + j(f/f_H)} Vin}$$

$$\therefore \frac{V_0}{Vin} = \left(1 + \frac{R_f}{R_1}\right) \cdot \frac{1}{1 + j(f/f_H)}$$

$A_F = 1 + \frac{R_f}{R_1}$ = passband gain

$$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j(f/f_H)}$$

1. at very low freqⁿ, $f < f_H$

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F$$

2. At $f = f_H$

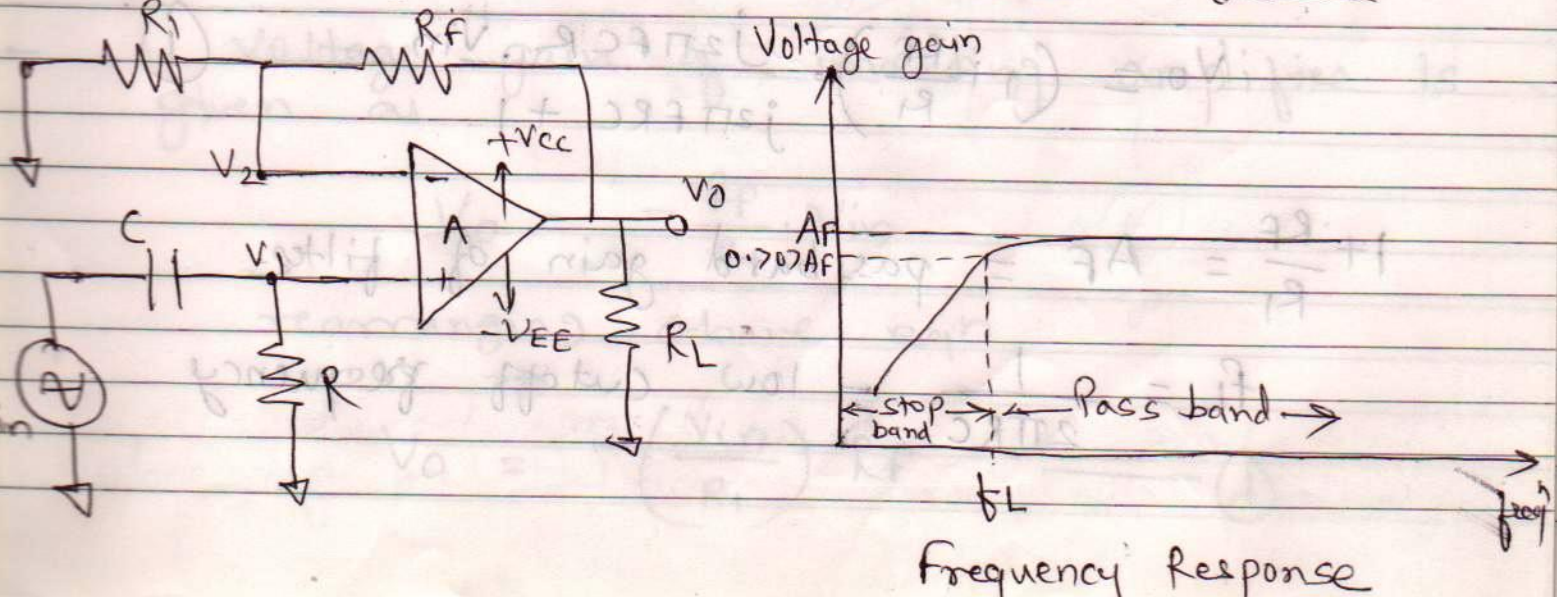
$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}}$$

3. At $f > f_H$

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$



## Active high pass Butterworth filter :



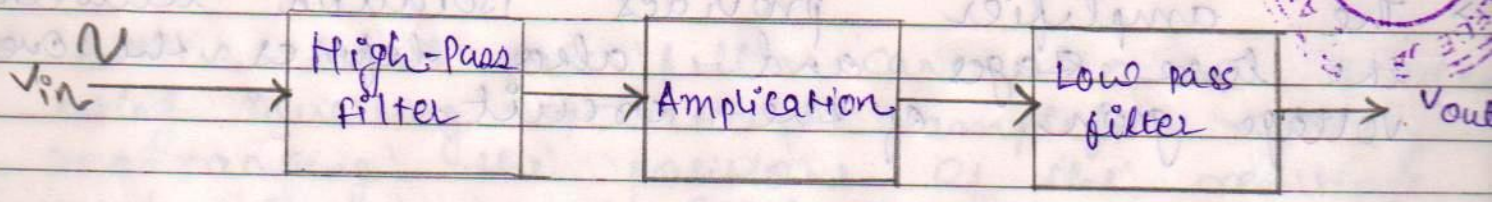

Frequency Response

Q Describe band pass active filter using operational amplifier with necessary diagram and equations.

→ The principal characteristic of a Band pass filter is its ability to pass frequencies over a specified band or band of frequencies called the "pass Band".

→ For the Active Band pass filter the band or range of frequencies is set between two cut-off or corner frequency points labelled the "lower frequency" ($f_L$) and the "higher frequency" ($f_H$) while attenuating any signals outside of these two points.

→ Simple Active Band pass filter can be easily made by cascading together a single low pass filter with a single High filter as shown.




→ One way of making a very simple Active Band pass filter is to connect the basic passive high and low pass filter to an amplifying op-amp circuit as shown.

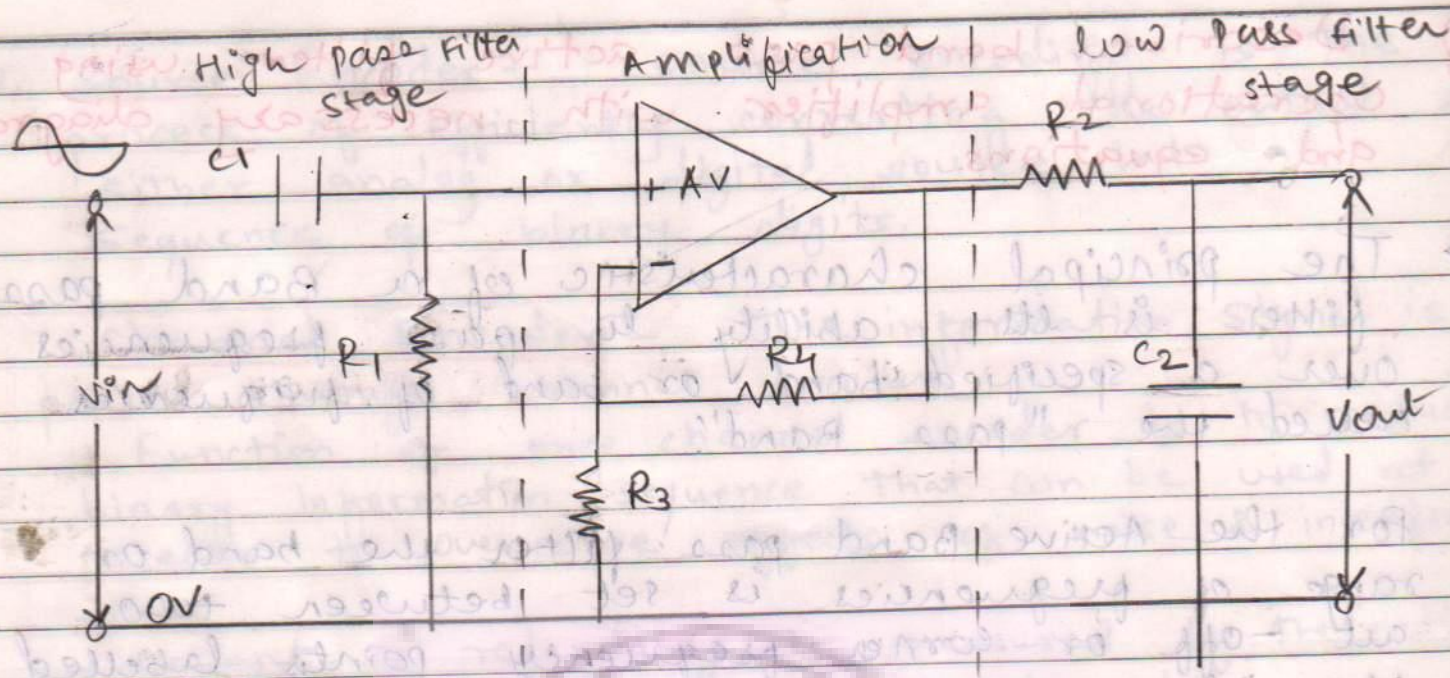


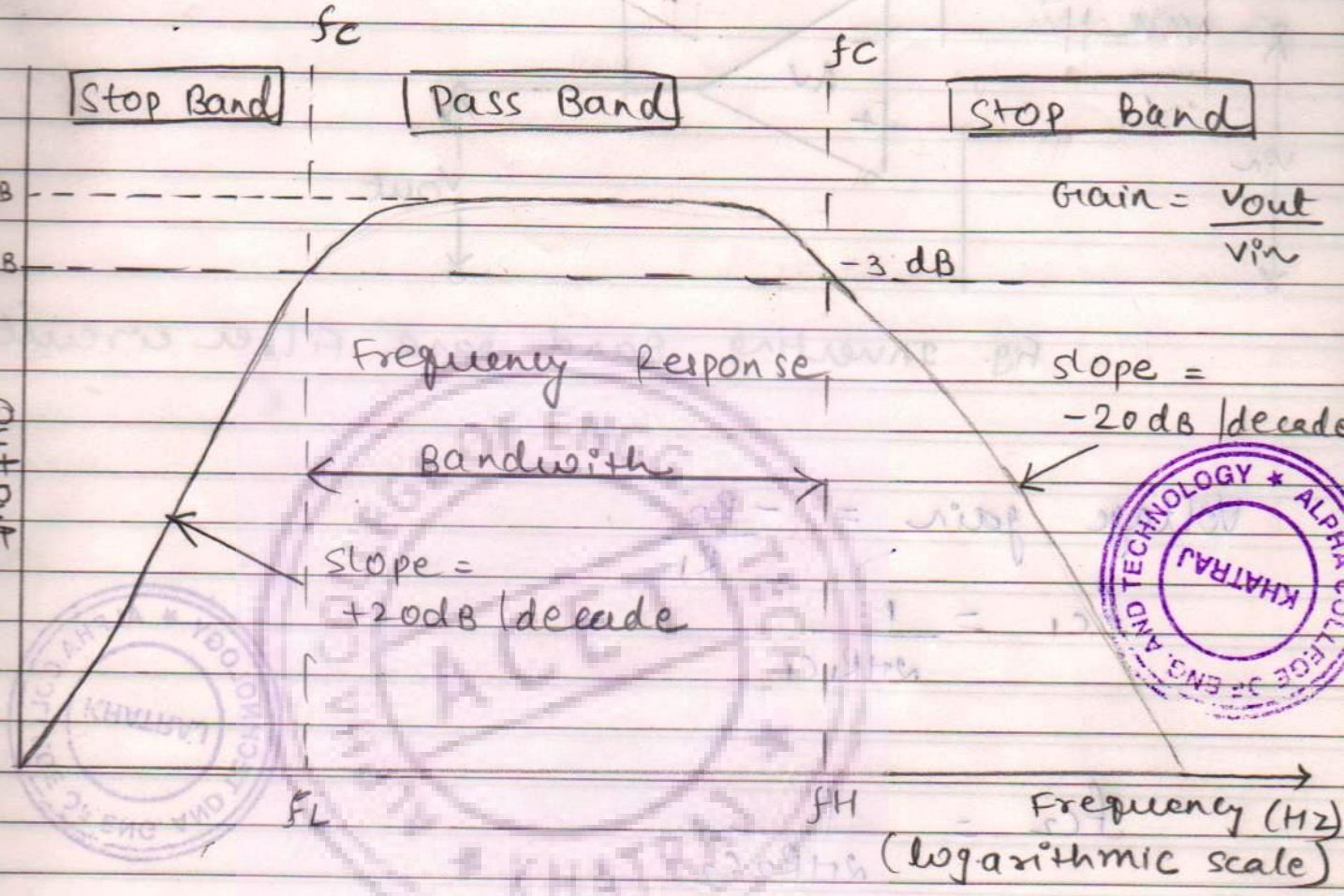

Fig. Active Band pass Filter circuit.

→ The Q factor relates to the "sharpness" of the resonance in a series resonance circuit. The sharpness of the peak is measured quantitatively and is called the quality factor, Q of the circuit.

→ The amplifier provides isolation between the two stages and also defines the overall voltage gain of the circuit.

→ The bandwidth of the filter is therefor the difference between these upper and lower -3 dB points.

→ The normalised frequency response for an active band pass filter will be as below.




→ Active band pass filter can also be made using inverting operational amplifier. So by rearranging the positions of the resistors and capacitors within the filter we can produce a much better filter circuit as shown below. For an active band pass filter, the lower cut off -3dB point is given by $f_{c2}$ while the upper cut-off -3dB point is given by $f_{c1}$.

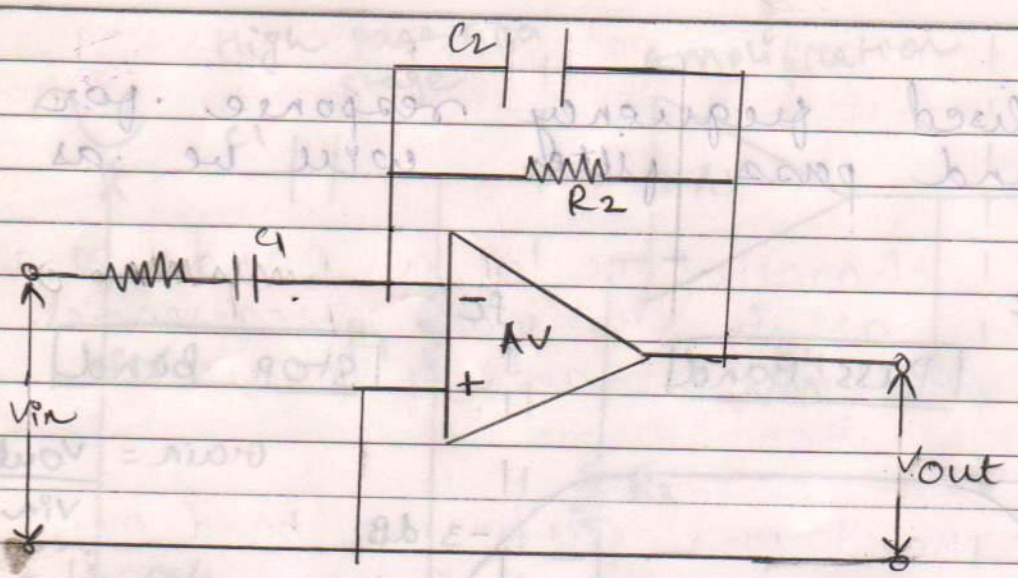



Fig. Inverting Band pass Filter circuit

Voltage gain $= \frac{-R_2}{R_1}$,

$$f_{c_1} = \frac{1}{2\pi R_1 C_1}$$

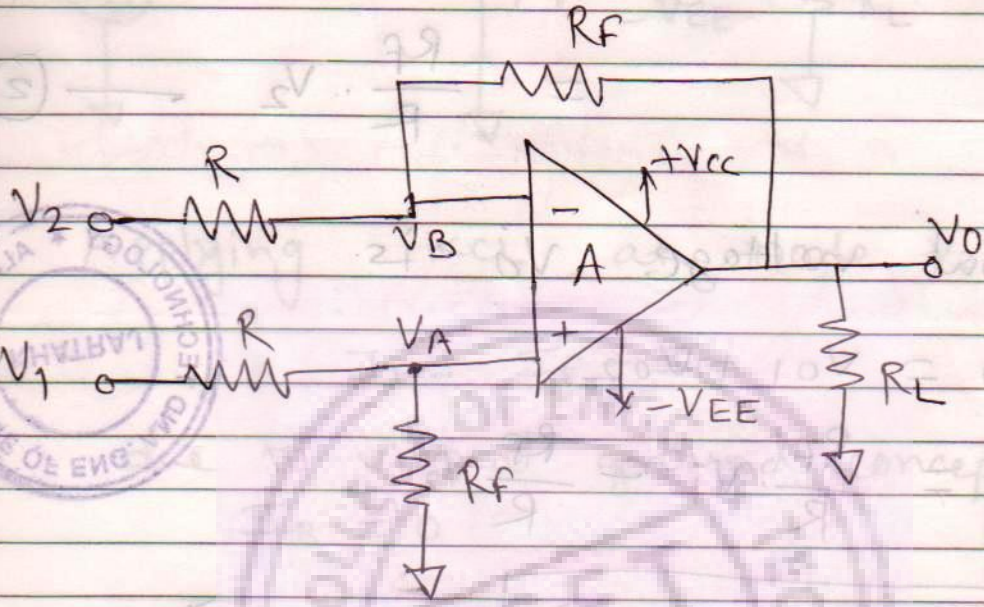
$$f_{c_2} = \frac{1}{2\pi R_2 C_2}$$



→ This type of band pass filter is designed to have a much narrower pass band. The center frequency and bandwidth of the filter is related to the values of $R_1$, $R_2$, $C_1$ and $C_2$.

$$V_o = V_1 + V_2 + V_3 \quad \text{---(3)}$$

## Differential Amplifier as a Subtractor (Summer - I






Total output voltage is equal to $V_{o1} + V_{o2}$ i.e using superposition the

Considering voltage $V_1$, op-amp is in non-inv. configuration

Output voltage $V_{o1} = \left(1 + \frac{Rf}{R_1}\right) \cdot V_A$

$$= \left(1 + \frac{Rf}{R_1}\right) \cdot \frac{V_1 \cdot Rf}{(R + Rf)}$$

$$= \left(1 + \frac{Rf}{R}\right)\left(\frac{Rf}{R + Rf}\right) V_1 \quad (\text{here } R_1 =$$

$$= \frac{Rf}{R} \cdot V_1 \quad \text{---(1)}$$

considering voltage ~~at~~ $V_2$, Op-amp works in inverting mode

$\therefore$ output voltage $V_{O2} = -\frac{R_f}{R_1} \cdot V_2$

$= -\frac{R_f}{R} \cdot V_2$ —— (2)

Total output voltage $V_O$ is

$V_O = V_{O1} + V_{O2}$

$= \frac{R_f}{R} \cdot V_1 - \frac{R_f}{R} V_2$

$$\boxed{V_O = \frac{R_f}{R}(V_1 - V_2)} \quad \text{—— (3)}$$

## Integrator :

- Circuit in which output voltage waveform is integration of the input voltage waveform is called integrating amplifier or integrator.
- feedback resistor $R_f$ is replaced by capacitor $C_f$.

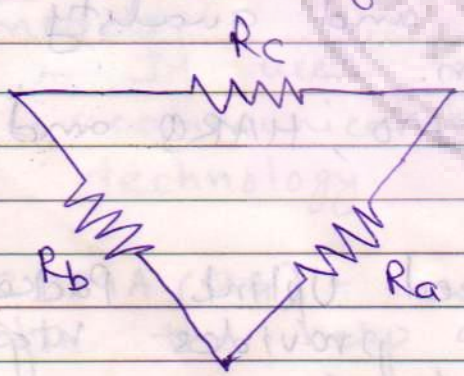
Q. Explain WYE-DELTA transformation in brief with necessary equations and circuit diagram.

AND

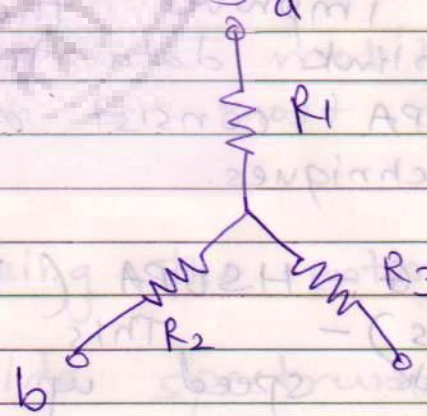
Explain DELTA - WYE transformation in brief with necessary equations and circuit diagram.

→ Many times in circuit analysis, resistors are neither connected in parallel or in series.

- Such circuits can be simplified by using three termind networks.
- These are the wye (Y) ~~or~~ and delta (Δ) networks.
- Δ & Y are used in three phase networks, electrical filters and matching networks.

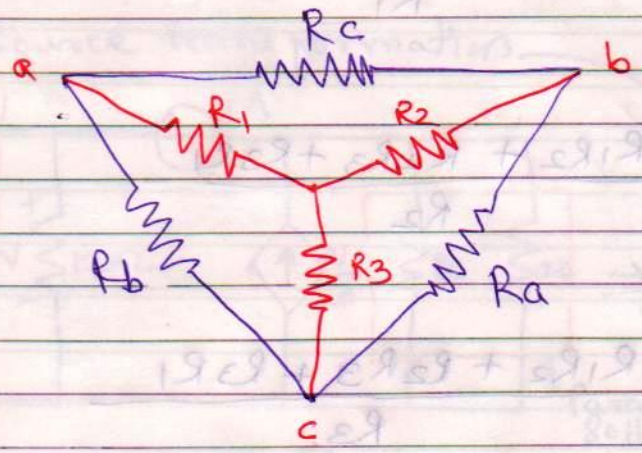



Delta network




star network

1. conversion of Delta to Wye connection:




Each resistor in the Y network is the product of the resistors in the two adjacent Δ branches divided by the sum of the three Δ resistors.

$$R_1 = \frac{R_b R_c}{R_a + R_b + R_c} \quad \text{——— (1)}$$

$$R_2 = \frac{R_c R_a}{R_a + R_b + R_c} \quad \text{——— (2)}$$

$$R_3 = \frac{R_a R_b}{R_a + R_b + R_c} \quad \text{——— (3)}$$

2. conversion of Wye to Delta connection:

Each resistor in the Δ network is the sum of all possible products of Y resistors taken two at a time, divided by the opposite Y resistor.

$$R_a = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_1}$$

$$R_b = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_2}$$

$$R_c = \frac{R_1R_2 + R_2R_3 + R_3R_1}{R_3}$$

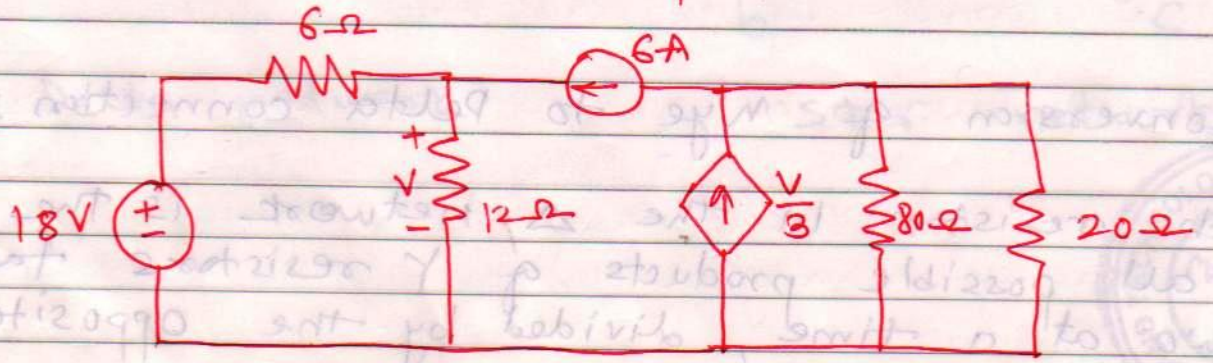
→ The Y & Δ networks are said to be balanced when

$R_1 = R_2 = R_3 = R_Y$ , $R_a = R_b = R_c = R_\Delta$

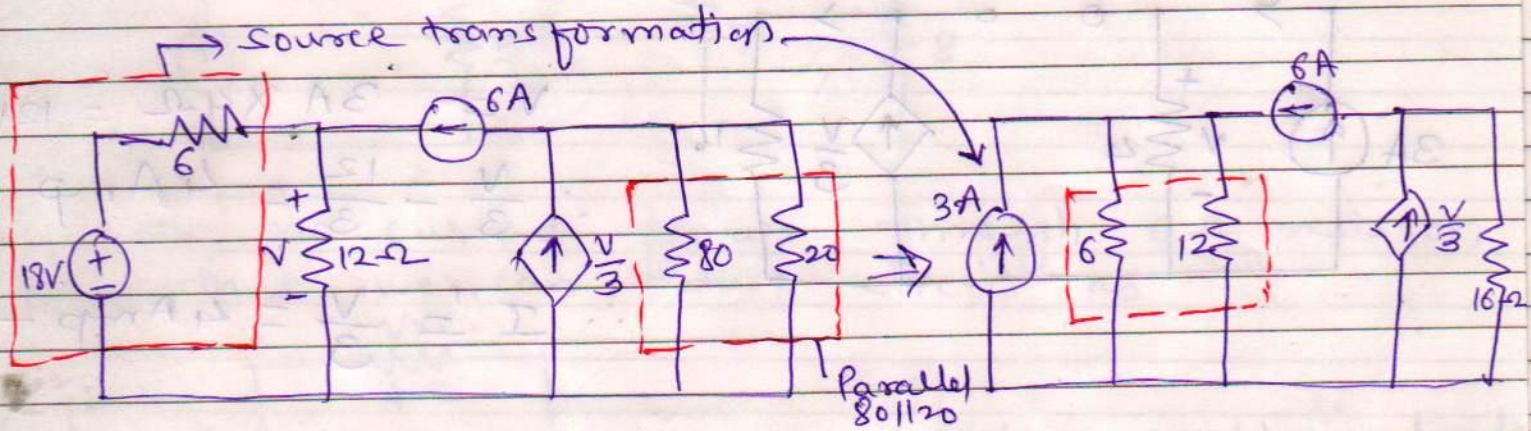
→ using this condition, conversion formulas become

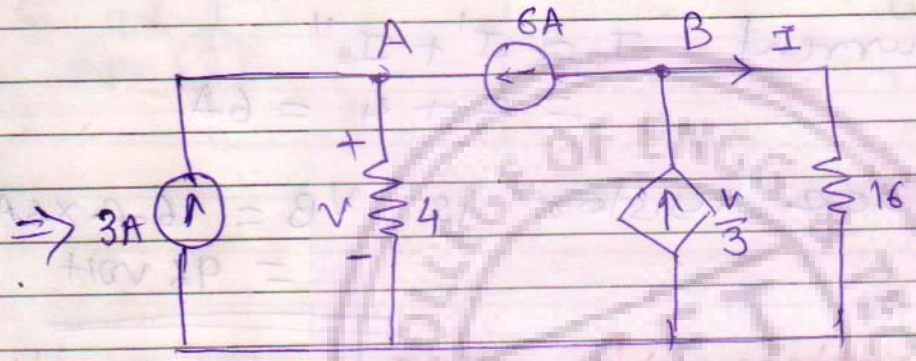
$$R_Y = \frac{R_\Delta}{3} \quad \text{or} \quad R_\Delta = 3R_Y$$

Q. Determine the voltage across the 20 Ω resistor in the circuit shown in fig. with the application of superposition Theorem.



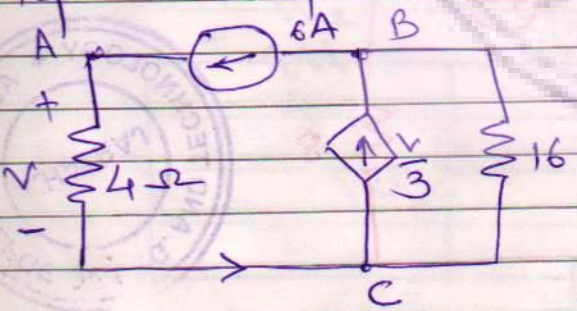
Step 1 : Simplify the given circuit




simplified circuit

Step 2 : Open circuit 3A source to find I'




from fig:

$V = 4 \times 6A$

$= 24$ volts

$\therefore \frac{V}{3} = \frac{24}{3} = 8$ Amp.

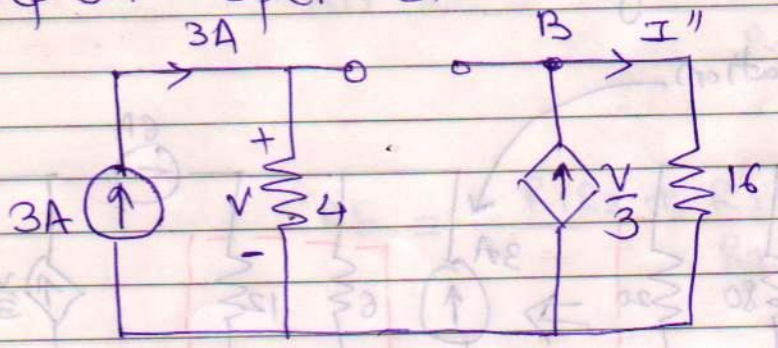
Step 3:

Applying KCL at node B,

$I' + 6A = \frac{V}{3}$ but $\frac{V}{3} = 8A$

$\therefore I' + 6 = 8 = 2A$ $\boxed{I' = 2A}$ — (1)

Step 3: Open circuit 6A source and find I".




$V = 3A \times 4\Omega = 12V$

$\therefore \frac{V}{3} = \frac{12}{3} = 4 Amp$

$\therefore I'' = \frac{V}{3} = 4 Amp$ — (2)

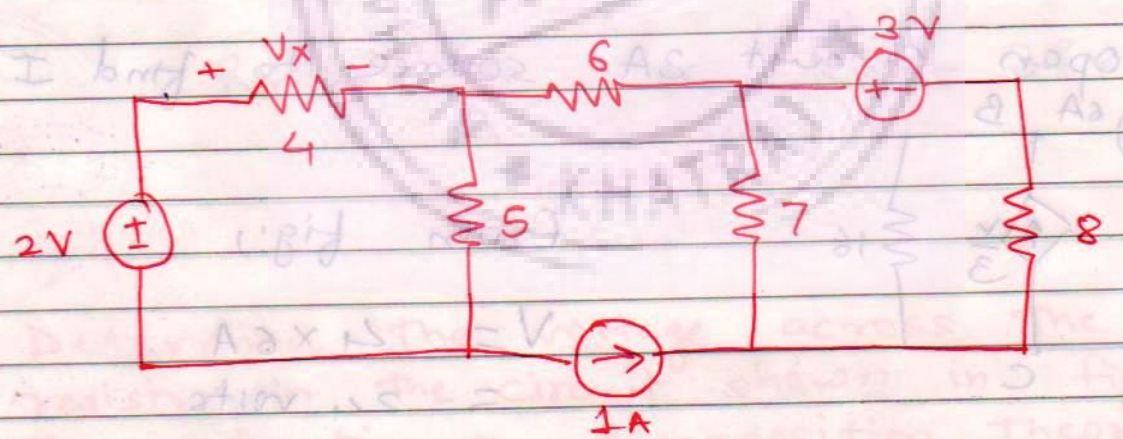
Step 4: Total current $I = I' + I''$

$= 2 + 4 = 6A$

∴ Voltage across 2Ω resistor is $V_B = 16\Omega \times 6A$

$= 96$ volt

Q. Find the voltage Vx using superposition theorem. All resistor values are in ohm.

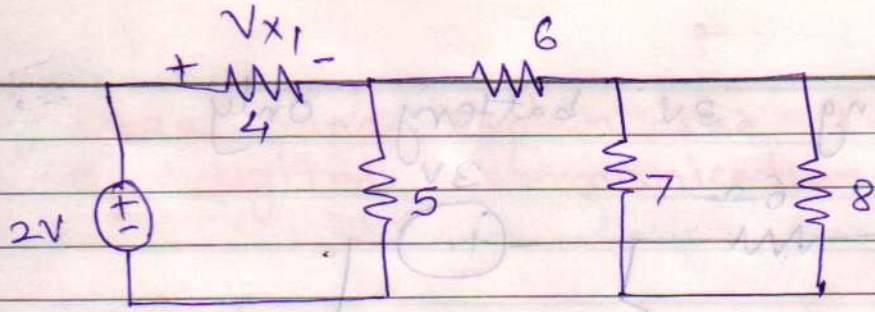




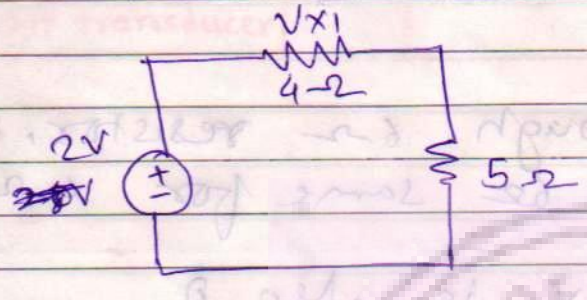

→ As there are three sources, voltage Vx can be found by solving three circuits

i.e $V_x = V_{x1} + V_{x2} + V_{x3}$

step 1: considering 2V source only replacing 3V as short & 1A as open




⇒ no current flows through 6Ω resistor, thus we can reduce circuit as

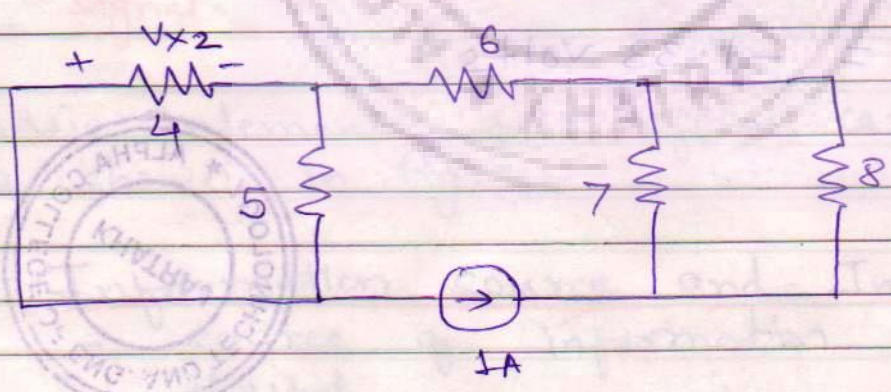



using voltage divider rule to find $V_x$

$$V_{x_1} = \frac{2 \times 4}{4+5}$$

$$= 0.89V \quad \text{---(1)}$$

Step 2: Considering 1A current source only, and short circuiting two voltage sources.



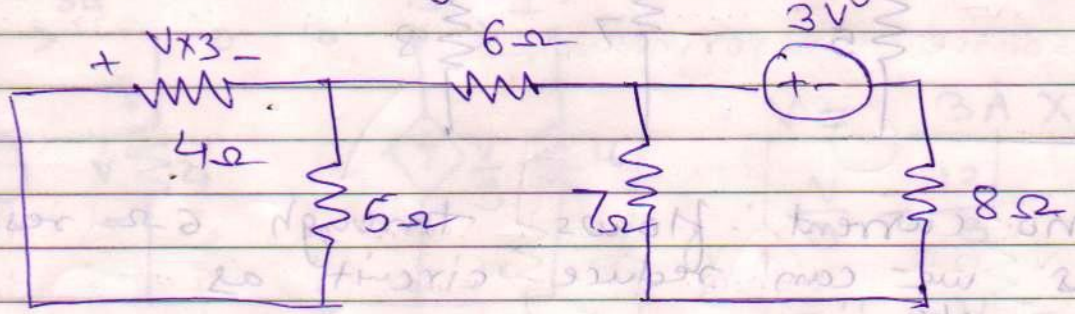



using current divider rule, current through 4Ω resistor is

$$I_{x_2} = \left(\frac{5}{4+5}\right) 1 = 0.56 \text{ Amp.}$$

$$\therefore V_{x_2} = -0.56 \times 4 = -2.22V \quad \text{---(2)}$$

Step 3 : considering 3V battery only




No current flows through 6Ω resistor, as no current through 6Ω same for 4Ω & 5Ω resistor.

∴ $V_{x3}$ due to 3V is also 0.

$$\therefore V_{x3} = 0 \quad \longrightarrow (3)$$

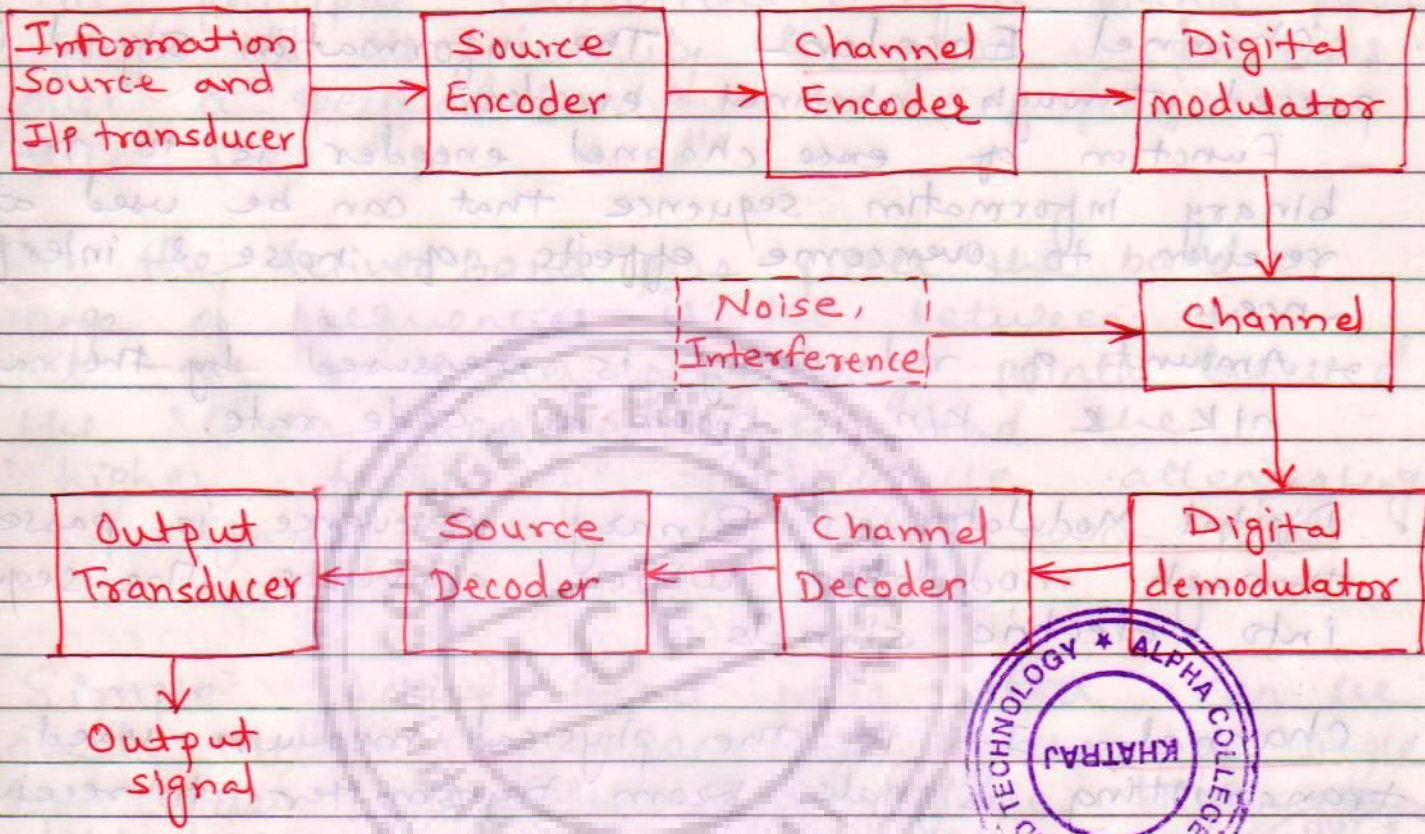
Total $V_x = V_{x1} + V_{x2} + V_{x3}$ (from eqn ①, ② & ③)

$= 0.89 + (-2.22) + 0$

$V_x = -1.33$ volts

Q. Draw and explain the functional description of digital communication system in brief.

→






→ Basic elements of digital communication system are shown in fig.

→ 1. Information source and Input Transducer:
- source of information can be analog or digital.
- examples of analog signals are audio or video signals
- examples of digital signal is tele type signal.
- In digital comm$^n$ the signal produced by this source is converted into digital signals consist of 1's and 0's.

2. Source Encoder – source encoding is the process of efficiently converting the output of either analog or digital source into a sequence of binary digits.

3. Channel Encoder – The information signal is passed through channel encoder.
- Function of channel encoder is to reduce binary information sequence that can be used at receiver to overcome effects of noise & interference.
- Amount of redundancy is measured by the ratio n/k & k/n is known as code rate.

4. Digital Modulator – Binary sequence is passed through modulator which converts the sequence into electric signals.

5. Channel – It is the physical medium used for transmitting signals from transmitter to receiver.

6. Digital Demodulator – It processes the channel corrupted transmitted waveform and reduces the waveform to the sequence of numbers.

7. Channel Decoder – output of demodulator is passed through decoder which reconstruct the original information sequence.

8. Source Decoder – It tries to decode the sequence from the knowledge of the encoding algorithm.

9. Output Transducer – It gives the desired signal in desired format i.e analog or digital.

Q. Classify the standard based on 2G & 3G.

→ The present day mobile phones that we use have come a long way since the formation of mobile telephone services.

→ The mobile technology is broadly classified into generations (0G, 2G, 3G, 4G) where G stands for generation.

→ 0G is being the initial phase and 3G | 4G which is in use currently.

2G standards:

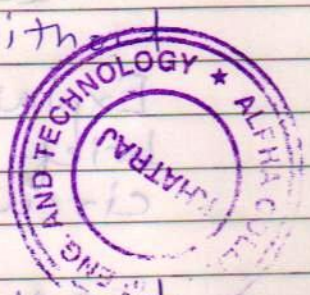
→ (1) GSM (2G) – Global system for mobile communication deals with digital signals.
- It has the facility of text messages, picture messages and video messages.

→ (2) TDMA (2G) – 2G mobiles uses Time division multiple access (TDMA) technology in some models.
- It uses global service mobile communication which is most common technology.

– (3) CDMA (2G) – works using the entire band with the help of code.
- CDMA based on wide spectrum.

– (4) 2.5 G – GPRS – General packet Radio service has higher capacity than 2G.
- GPRS adds packet switched capabilities and TDMA networking.
- It has features like WAP, email, MMS

- (5) 2.75 - EDGE (Enhanced Data Rates for GSM evolution) - It is an extended version of 2.5G.
  - It provides fast transmission without glitches.




3G Standards :

(1) IMT-2000 - From 3G era internet, email and other web features became associated with mobile phones.
  - This technology support data transfer rates upto 2Mbps and support multimedia applications.
  - It makes use of CDMA & TDMA technologies.

(2) 3.5G - HSDPA (High-Speed Downlink Packet Access) - It is a mobile telephony protocol which provides packet based services.
  - It improves the speed and quality of downlink data transmission.
  - HSDPA consist of MIMO, HARQ and AMC techniques.

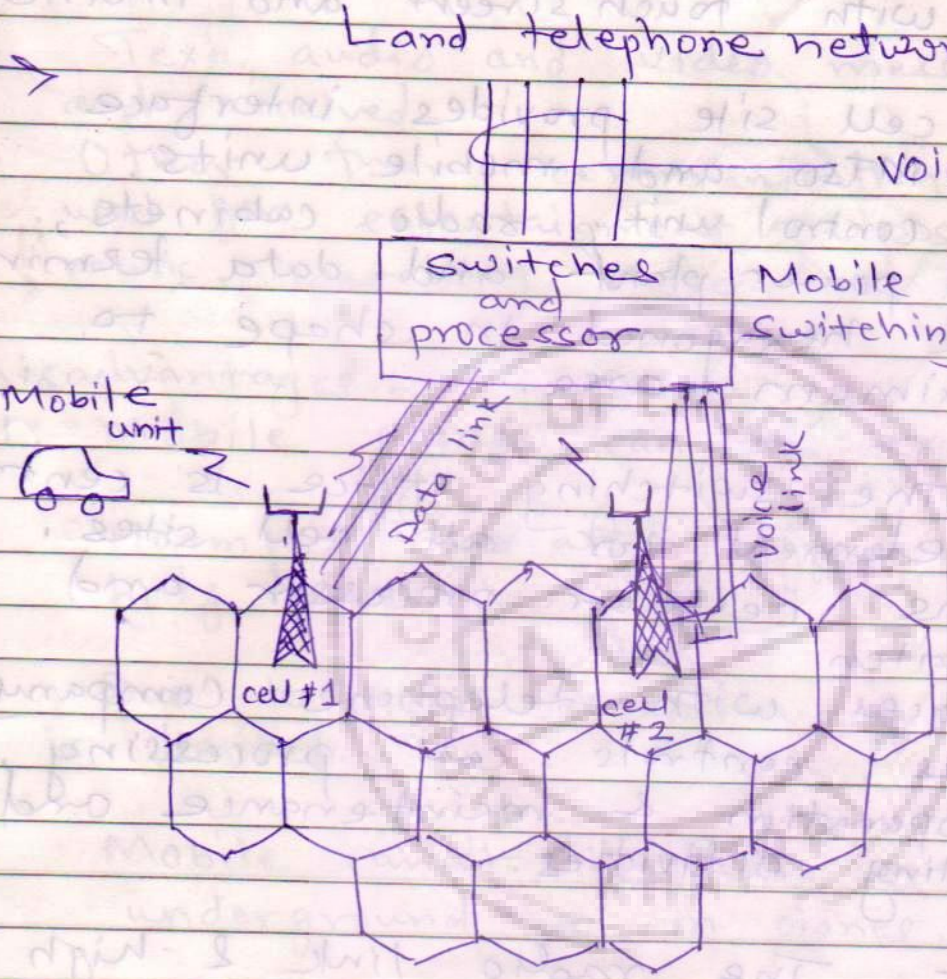
(3) 3.75 G - HSUPA (High speed Uplink Packet Access) - This protocol provides higher uplink speed up to 5.8 Mbps.
  - HSUPA works on request grant principle.
  - HSUPA enhances the uplink speed by increasing throughput, capacity & decreasing delays.

Q. Explain in brief cellular concept in mobile radio system

OR

Write short note on cellular communication system

→




Basic cellular system



- cellular phone communication system operates in the area divided into small cells and called as cellular communication.
- A basic cellular system consists of three subsystems :
  1. a mobile unit (handset / mobile phone)
  2. a cell site (hexagonal in shape)
  3. Mobile telephone switching office (MTSO).

1. Mobile unit – A mobile telephone is a transceiver.
   - Now days mobile units are mostly smart phones.
   - Smart phones performs many functions of a computer with touch screen and internet.

2. Cell site – cell site provides interface between the MTSO and mobile units.
   - It has a control unit, radio cabinets, antennas, a power plant and data terminals.
   - cell site are hexagonal in shape to cover maximum area.

3. MTSO – The switching office is central co-ordinating element for all cell sites.
   - It contains cellular processor and cellular switch.
   - It interfaces with telephone company zone offices, controls call processing, provides operation & maintenance and handles billing activities.

4. Connections – The radio link & high frequency links connect the three subsystems.
   - each mobile unit can only use one channel at a time for its communication link.

- MTSO is the heart of the cellular mobile system.
- Cellular switch can be either analog or digital.

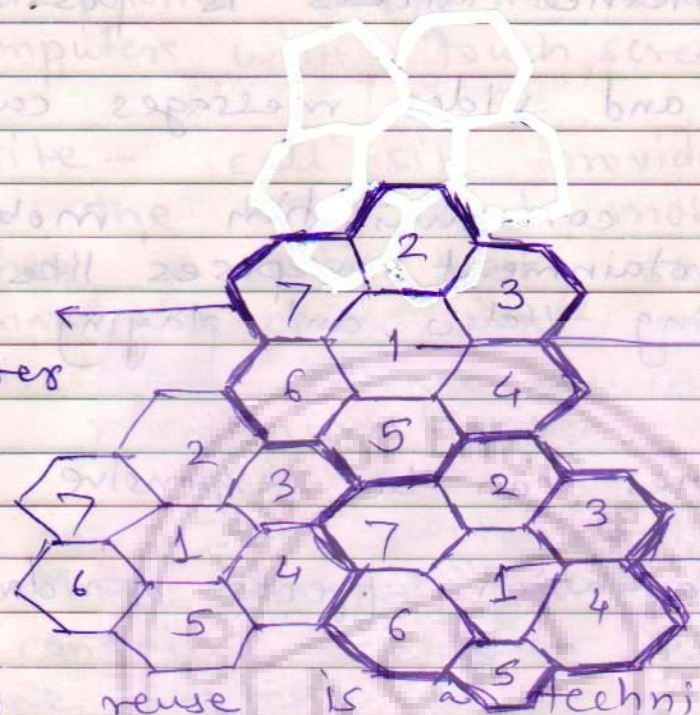
Advantages:

1. communication is possible almost 24/7 and anywhere in the world.
2. constant Internet access is possible.
3. Text, audio and video messages can be sent and received.
4. Other than communication, mobile can be used for entertainment purposes like listening music, watching video and playing games etc.

Disadvantages:

1. Mobile phones can be expensive
2. Harmful radiation effects or damage body parts.
3. Due to poor reception of signal, connectivity is limited.
4. Mobile can't be use everywhere e.g. underground or in planes.

Q. What do you understand about frequency reuse concept & why it is used in cellular system?




- Frequency reuse is a technique of rewing frequencies and channels within a communication system to improve capacity and spectral efficiency.
- Frequency reuse in mobile cellular systems means that frequencies allocated to the service are reused in a regular pattern of cells, each covered by one base station.
- The repeating regular pattern of cells is called cluster.
- Since each cell is designed to use radio frequencies only within its boundry, the same frequencies can be reused in other cells without interference in another cluster.
- Such cells are called co-channel cells.
- The reuse of frequencies enables a cellular system to handle a hage number of calls with a limited number of channels.

- The closest distance between the co-channel cells is determined by the choice of the cluster size and layout of the cell cluster.
- consider cellular system with D duplex channels available for use & N - no. of cells in cluster.
- If each cell allotted E duplex channels

$$D = EN \quad \text{under normal conditions.}$$

- If cluster are repeated M times within the total area, total number of users in a system will be

$$T = MD = MEN$$

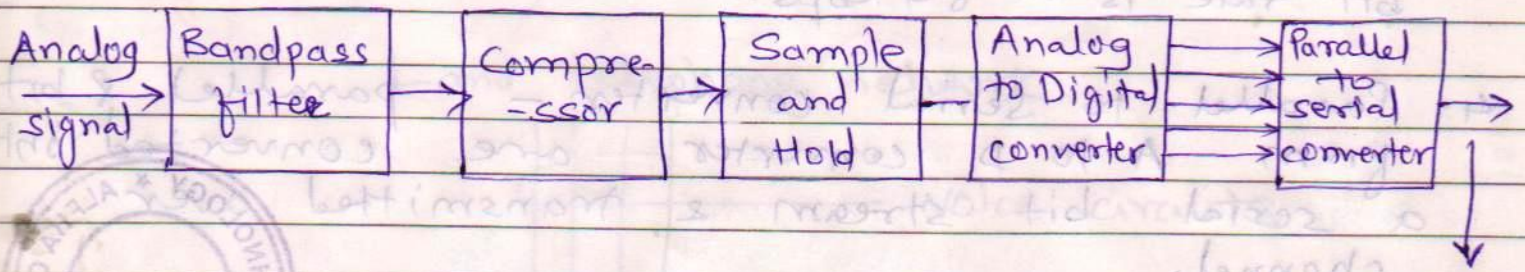
if E & N remain constant,

$$T \propto M$$

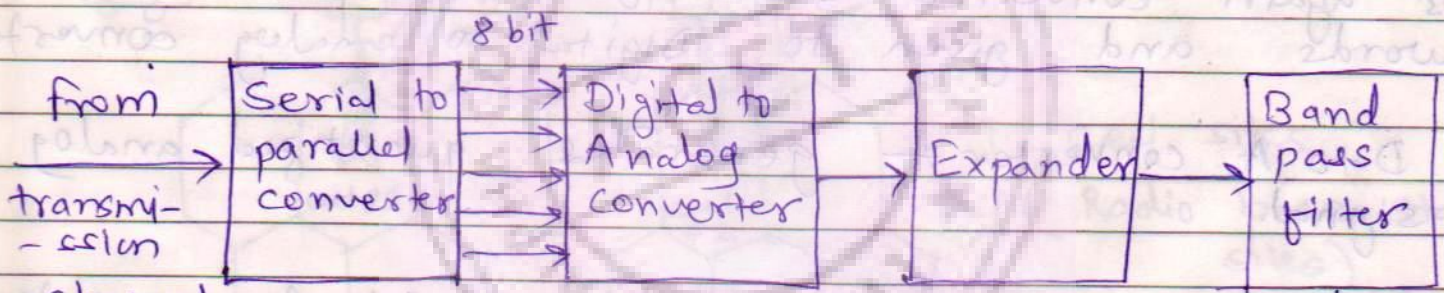
eqn shows that capacity gain achieved (T) is directly proportional to number of times a cluster is repeated (M).

Q. Draw block diagram of pulse code modulation

→




PCM Transmitter




PCM Receiver



PCM transmitter :

1. Bandpass filter – Design to pass only bandwidth of 300 Hz – 3.4 KHz.

2. Compressor – It converts smaller amplitude variations into larger one & vice versa.
   – Used to take care of weak signals so that SNR (signal to noise ratio) is not affected.

3. Sample & Hold - The compressed analog signal is sampled and converted into digital code word of eight bits.
- The sampling rate is 8 KHz so that total bit rate is 64 kbps.

4. Parallel to serial converter - parallel 8 bit from A to D converter are converted into a serial bit stream & transmitted over channel.


PCM Receiver:

1. serial to parallel converter - serial bit stream is again converted back to 8-bit parallel code words and given to Digital to analog converter.

2. D to A converter :- generates quantized analog signal.

3. Expander - when output of D to A converter is given to expander, it will restore original signal amplitude which was changed by compressor.

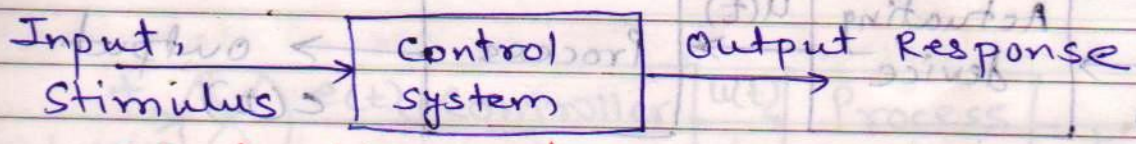
4. Band pass filter - This will ensure that original signal with bandwidth of 300 Hz - 3.4 KHz only passes through it.
- Analog output will be exact replica of original analog signal.

In PCM system, signal to noise ratio (SQNR) is defined as

$$SQNR = 2^{2N}$$

where N - no. of bits for a code word

Q. What is control system?




Simple block diagram of control system

→ Control system consist of subsystems and a process for controlling the output of the process.

→ Input is the stimulus, excitation or command applied to a control system.

→ Output is actual response resulting from a control system.

→ A control system gives output or response for given input or stimulus.

→ There are many examples of control system - bread toaster, power plant, launching a satellite, tracking an enemy plane on radar, ~~etc~~ robotics, ship and marine control etc.

Q. Explain types of control system.

Depending on the control action, system is divided into two types

1. Open-loop control system
2. Closed-loop control system.

Q. Compare open loop and closed loop control system.

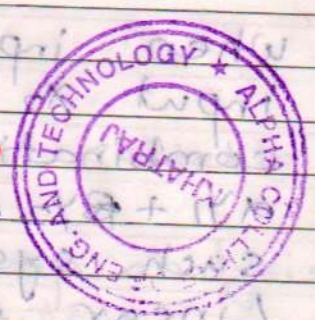


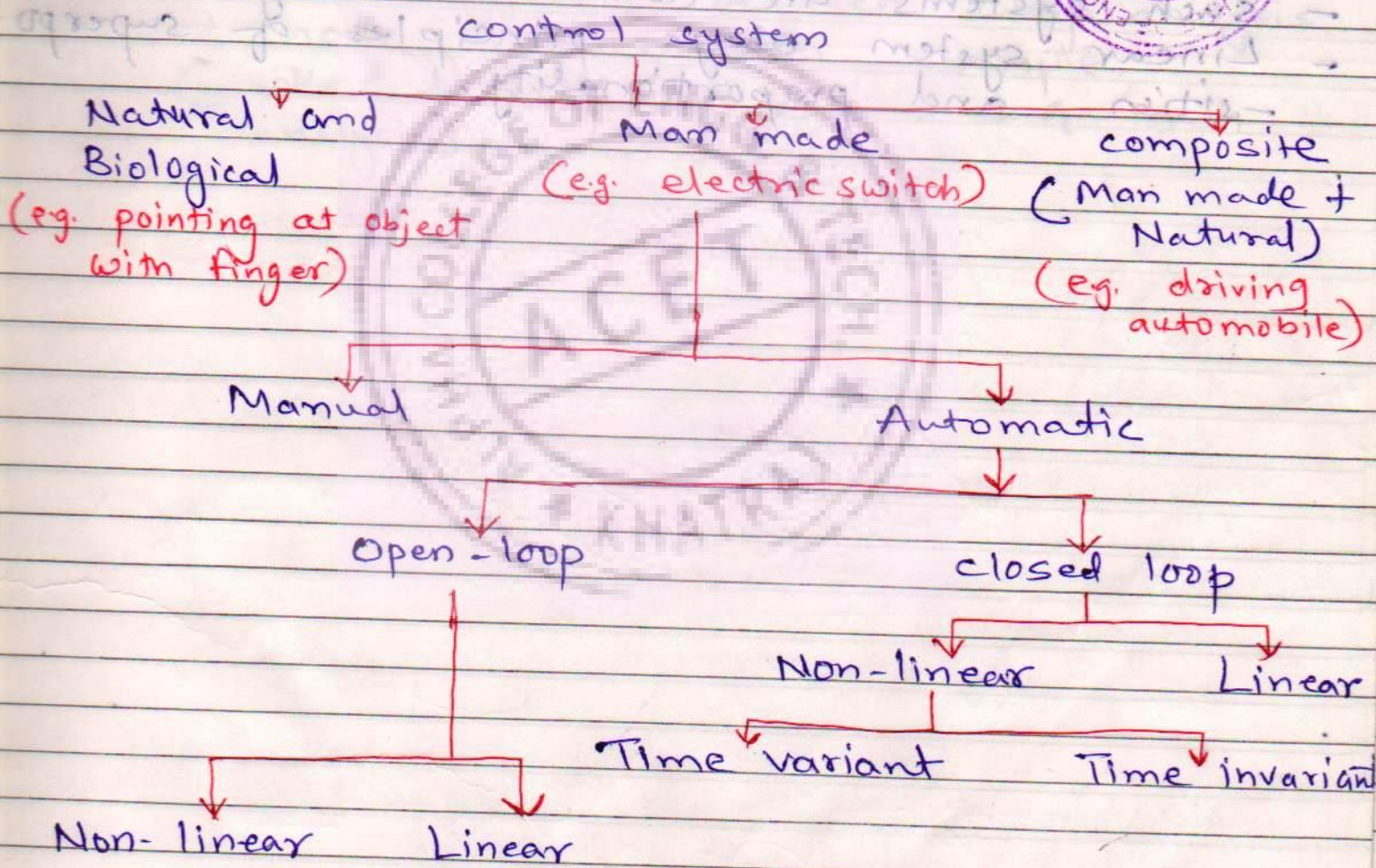
| | Open loop system | Closed loop system |
|---|---|---|
| 1. | System in which control action is independent of the output., no feedback is used. | System in which control action is depend on output, hence feedback is used. |
| 2. | Simple to construct and cheap. | complicated to construct and costly. |
| 3. | Open loop systems are generally stable. | closed loop systems can become unstable under certain condition. |
| 4. | Highly sensitive to disturbances and environmental changes. | Less sensitive to disturbances and environmental changes. |
| 5. | Error detector is absent. | Error detector is necessary. |
| 6. | Bandwidth is small. | Bandwidth is large. |
| 7. | Error detector is not there. | Error detector is necessary. |
| 8. | Feedback element is absent | Feedback element is present. |
| 9. | These systems are slow | These systems are faster. |

10. open loop systems are not reliable
closed loop systems are more reliable.

11. e.g. coffee maker, automatic toaster, hand drier.
e.g. Guided missile, servo voltage stabilizer.

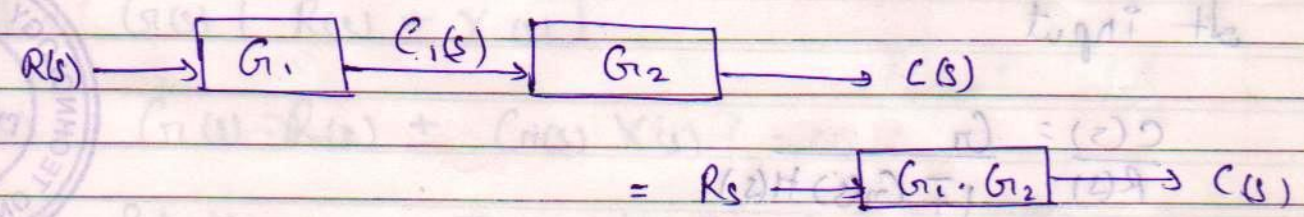
Q- Classify the control system



Q. Explain any four rules of Block diagram reduction for control system with necessary block diagrams.

**Rule -1** : Combining Blocks in Cascade (series)




At Input =

$$C(s) = C_1(s)\, G_2 \quad \text{—(1)}$$

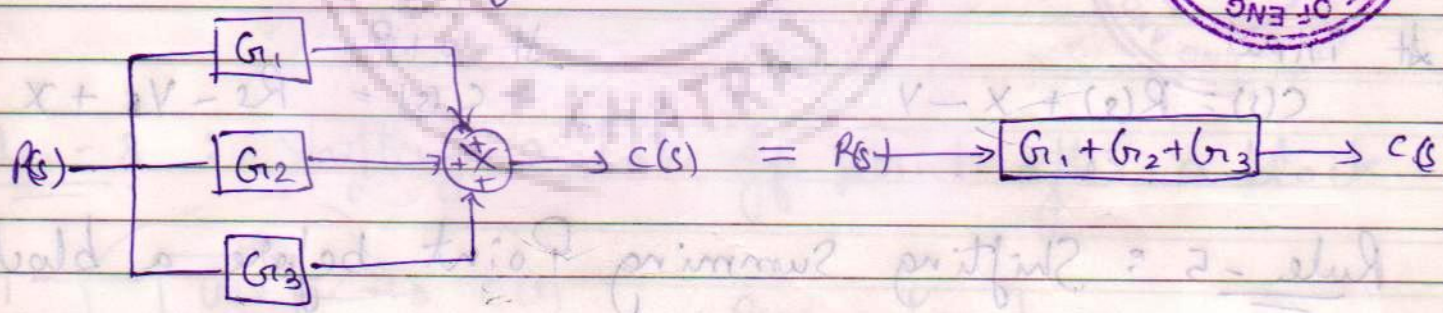
$$C_1(s) = G_1\, R(s) \quad \text{—(2)}$$

combining (1) and (2)

$$C(s) = [G_1 . G_2]\, R(s) \quad \text{—(3)}$$

$$\frac{C(s)}{R(s)} = G_1 . G_2 \quad \text{—(4)}$$

**Rule -2** : Combining Blocks in Parallel



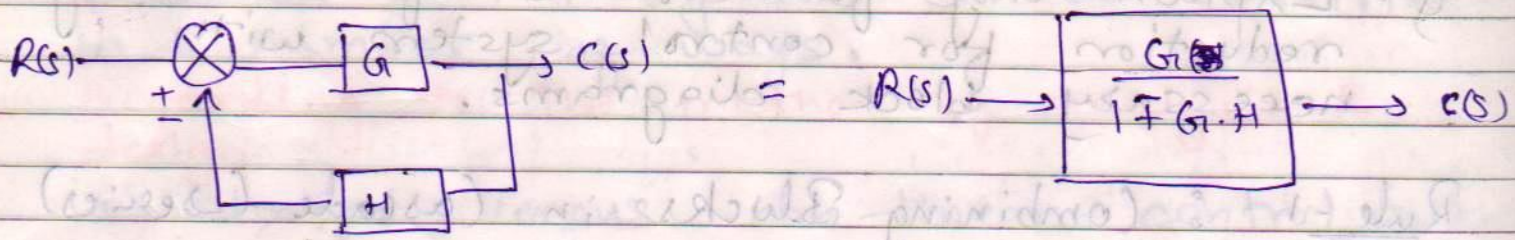

At input

$$C(s) = G_1 R(s) + G_2 R(s) + G_3 R(s) \quad \text{—(1)}$$

$$C(s) = R(s)\,[G_1 + G_2 + G_3] \quad \text{—(2)}$$

$$\therefore \frac{C(s)}{R(s)} = G_1 + G_2 + G_3 \quad \text{—(3)}$$

## Rule - 3 : Eliminating Feedback loop

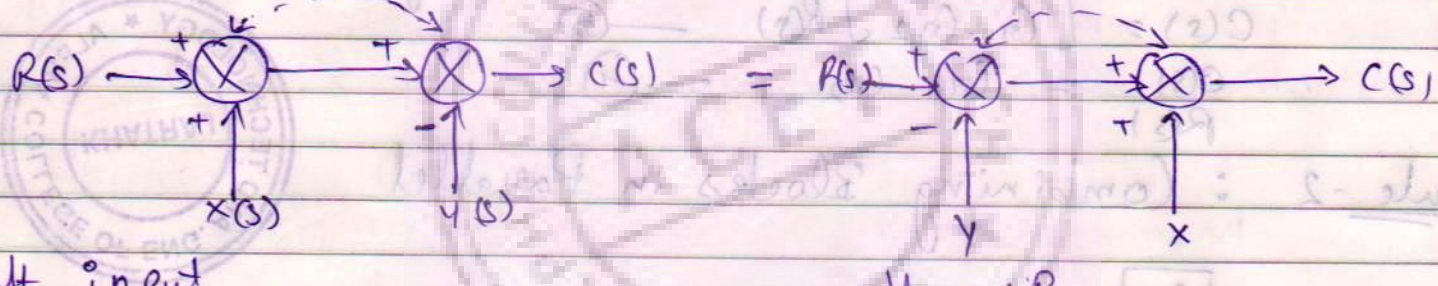



At input

$$\frac{C(s)}{R(s)} = \frac{G}{1 \mp G(s)H(s)}$$



## Rule - 4 : Interchanging of Summing Point or Associative Law



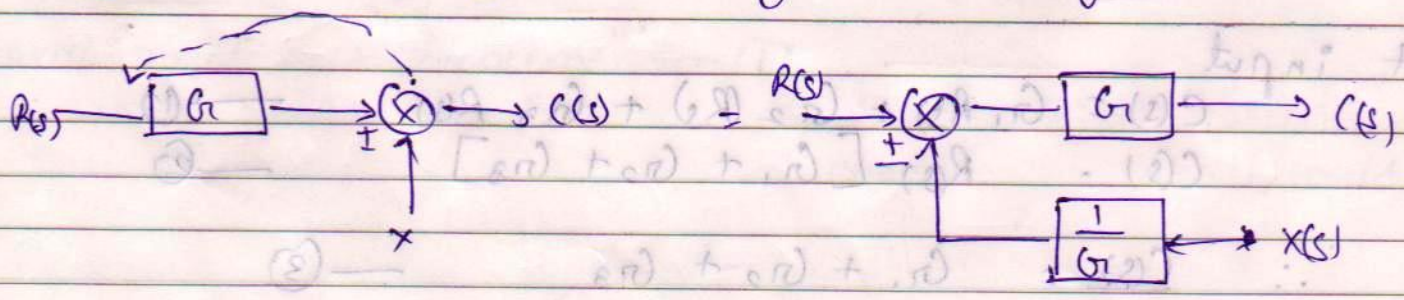

At input

$$C(s) = R(s) + X - Y$$

At o/p

$$C(s) = R_s - Y_s + X$$

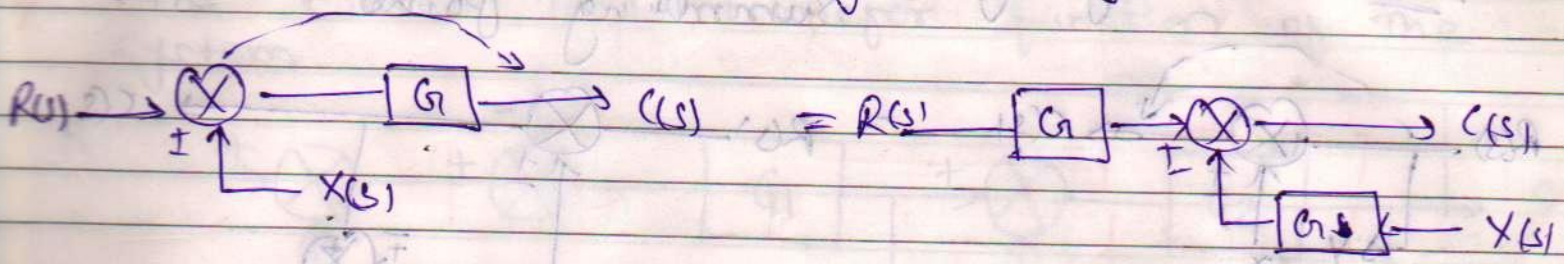
## Rule - 5 : Shifting Summing Point before a block




$$C(s) = G(s)R(s) \pm X(s)$$

$$= G(s)\left[R(s) \pm \frac{1}{G(s)} X(s)\right]$$

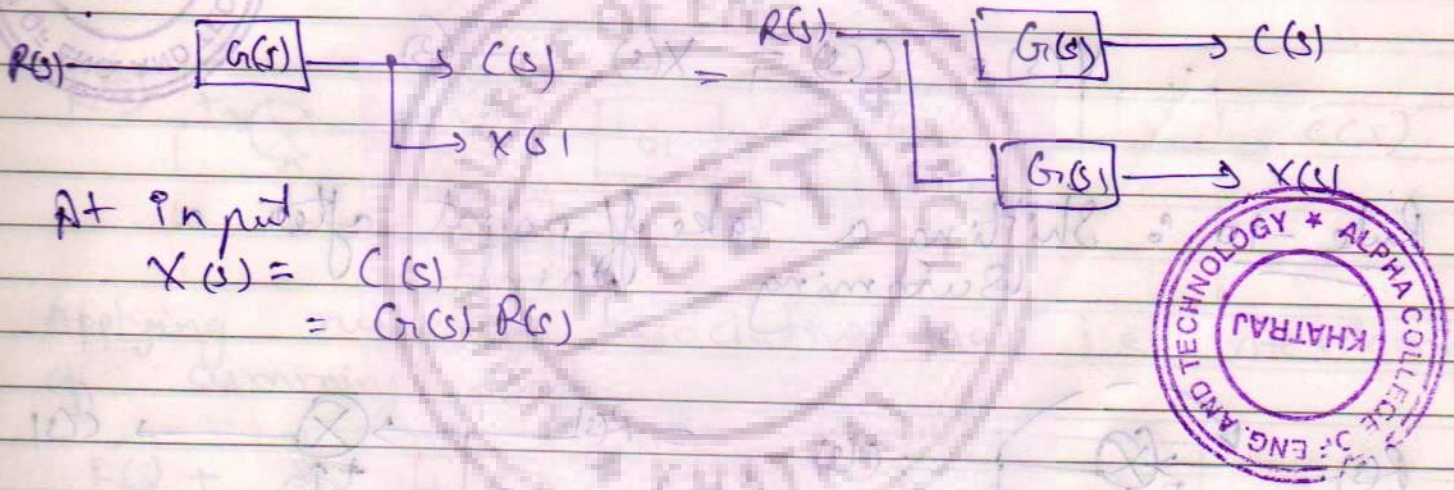
## Rule-6 : Shifting a Summing Point after a Block




$$C(s) = G(s)\,[R(s) \pm X(s)]$$

$$C(s) = G(s)\,R(s) \pm G(s)\,X(s)$$

## Rule-7 : Shifting a Take off Point before a block



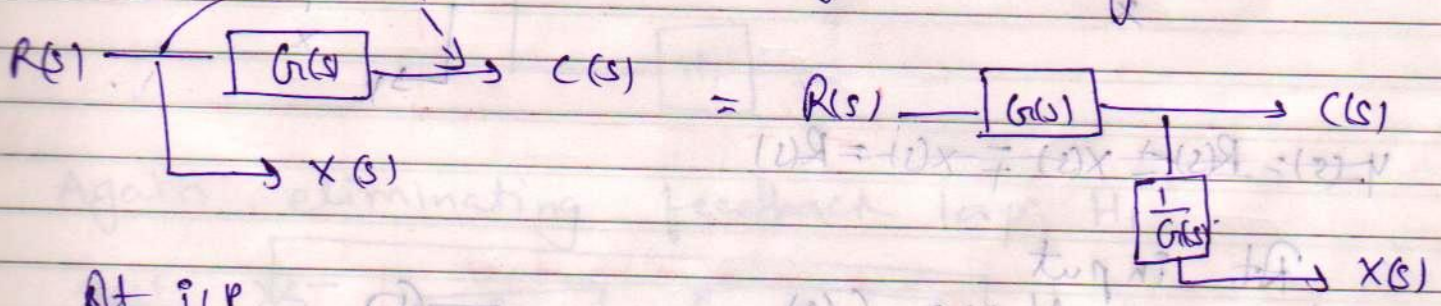

At input

$X(s) = C(s)$

$= G(s)\,R(s)$



## Rule-8 : Shifting a take off point after a block

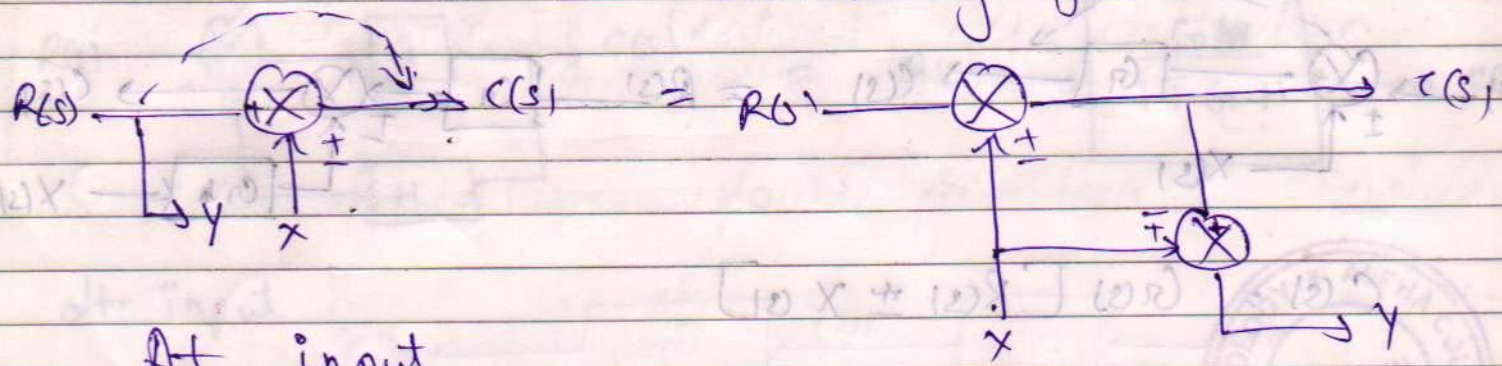



At i/p

$X(s) = R(s)$ ; $X(s) = \frac{1}{G(s)}\,C(s)$

and $C(s) = G(s)\,R(s)$

## Rule - 9 : Shifting a Take off point after a Summing point




At input

$$Y(s) = R(s) \quad \text{—(1)}$$

Also

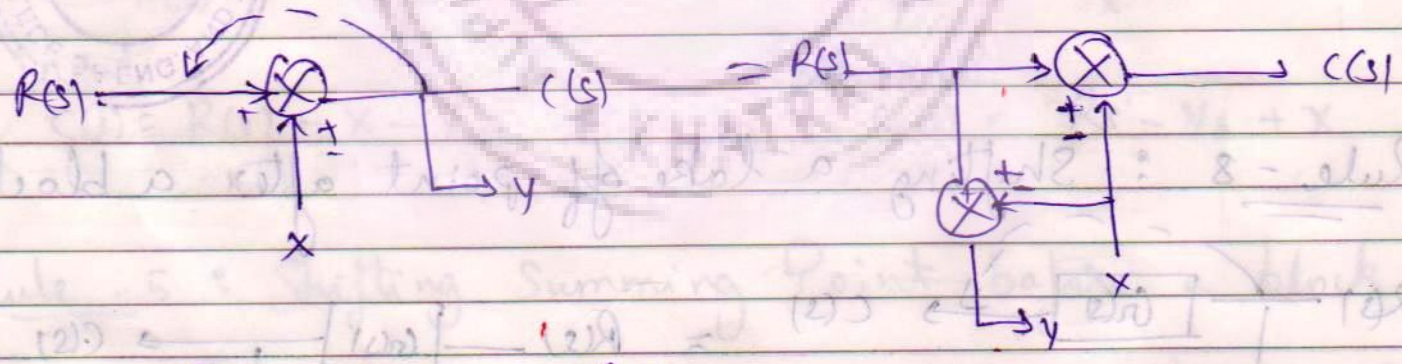
$$C(s) = R(s) \pm X(s) \quad \text{—(2)}$$

or $R(s) = C(s) \mp X(s)$

$$\therefore Y(s) = C(s) \mp X(s) \quad \text{—(3)}$$



## Rule - 10 : Shifting a Take off point after a Summing point



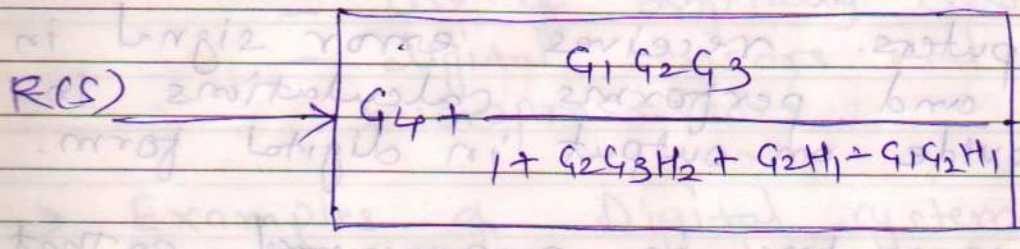

~~$Y(s) = R(s) \mp X(s) \mp X(s) = R(s)$~~

At input

$$Y(s) = C(s) \quad \text{—(1)}$$

$$= R(s) \pm X(s) \quad \text{—(3)}$$

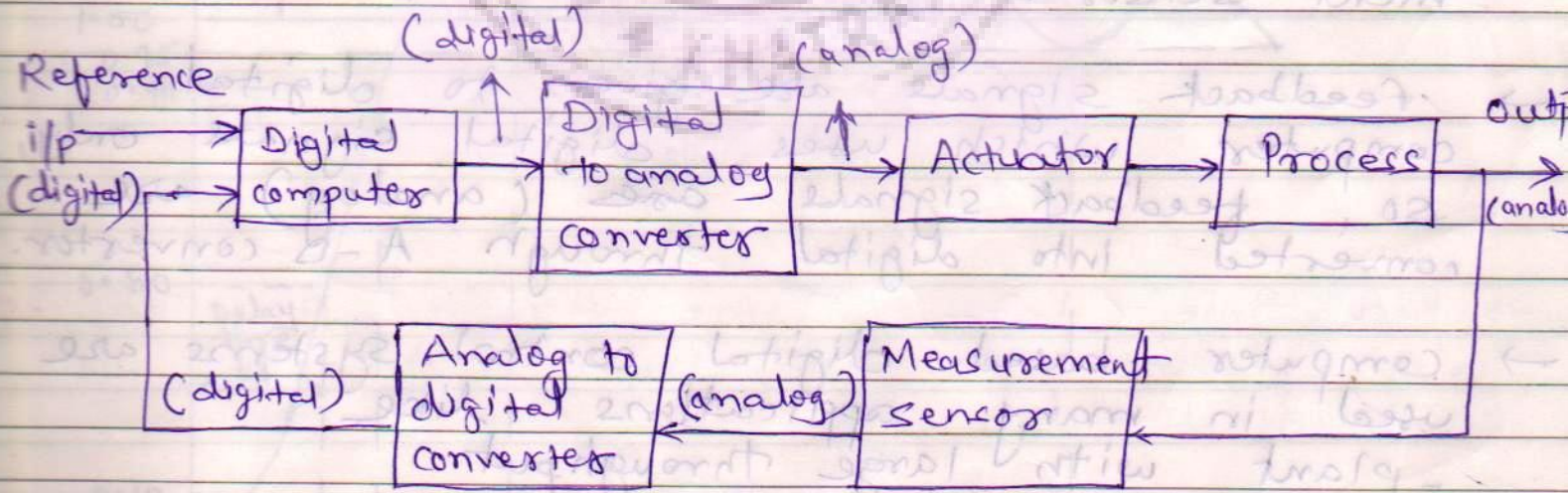
as two blocks are in parallel, using rule of parallel connection




$$\frac{C(s)}{R(s)} = G_4 + \frac{G_1G_2G_3}{1 + G_2G_3H_2 + G_2H_1 - G_1G_2H_1}$$

$$= \frac{G_4 + G_2G_3G_4H_2 + G_2G_4H_1 - G_1G_2G_4H_1 + G_1G_2G_3}{1 + G_2G_3H_2 + G_2H_1 - G_1G_2H_1}$$

Q. Explain Digital control system with necessary block diagram.




→ In digital control system, digital computers are used, to implement control system.

→ fig shows block diagram of a single loop digital control system.

→ Digital computers receives error signal in digital form and performs calculations in order to provide an output in digital form.

→ Output of computer is programmed so that we can get desired performance.

→ Output of digital computer which is digital signal given to D-A convertee.

→ Digital to analog converter, converts digital signals into analog signals.

→ Analog signals are further given to actuators and process.

→ Output of process is feedback to measurement sensor.

→ feedback signals are given to digital computer which uses digital signals only, so, feedback signals are (analog) are converted into digital through A-D converter.

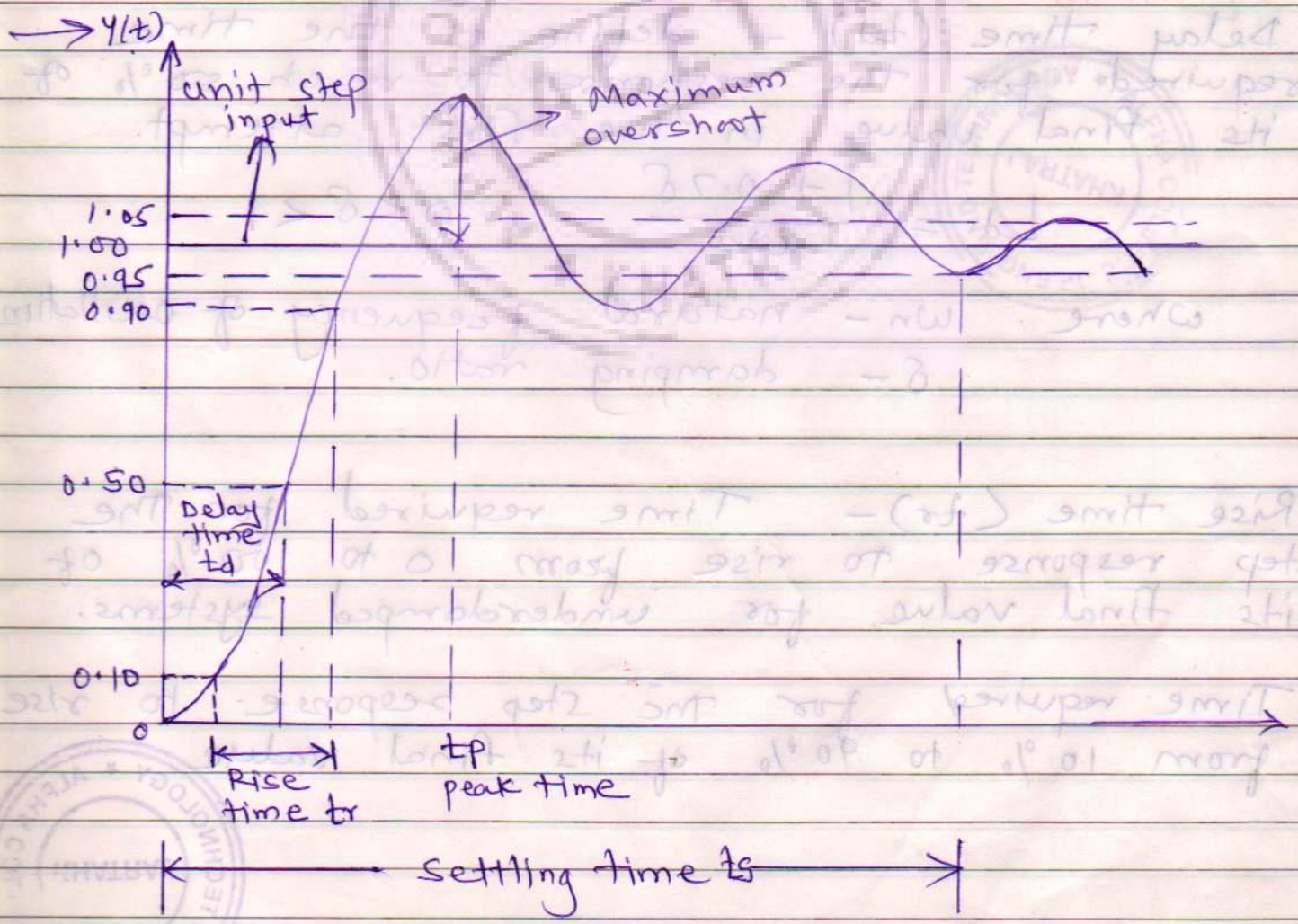
→ computer based digital control systems are used in many applications like
- plant with large throughput
- complex plant
- Batch processes
- New processes — plant with 40-50 control loops.

→ Advantages of digital control systems are
- improved measurement sensitivity
- use of digitally coded signals
- digital sensors and transducers and microprocessors.

→ Examples of Digital system are radar tracking system and a space satellite, metal working processes, chemical processes, aircraft control etc.



Q. Explain the typical unit step response (Transient response) of the control system.



→ The transient response of a system to a unit-step depends on the initial conditions.

→ It exhibits damped oscillations before reaching steady state.

→ The response of a control system when the input is a unit step function is called unit step response.

→ From figure, it is observed that the step response has a number of overshoots and undershoots with respect to the final steady value.

→ Delay time ($t_d$) – define as the time required for the response to reach 50% of its final value in the first attempt.

$$t_d = \frac{1 + 0.7\delta}{\omega_n} \qquad 0 < \delta < 1$$

where $\omega_n$ – natural frequency of oscillations
$\delta$ – damping ratio.

→ Rise time ($t_r$) – Time required for the step response to rise from 0 to 100% of its final value for underdamped systems.

Time required for the step response to rise from 10% to 90% of its final value

→ Peak time ($t_p$) - It is the time required for the response to reach the first peak.

→ Peak overshoot or Maximum overshoot ($M_p$) - It is the maximum deviation of the output over the step input during transient state.

→ Settling Time ($t_s$) - Time required for the step response to reach and stay within its final value.
$t_s$ is the largest time constant of the control system.

→ Steady state error ($e_{ss}$) - is define as the difference between the desired output and actual output as time tends to infinity.

$$e_{ss} = \lim_{t \to \infty} e(t).$$